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DESIGN AND OPTIMIZATION OF ENERGY EFFICIENT M-GDI BASED MAC UNIT USING FINFET TECHNOLOGY

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Abstract

This paper presents how the need for more efficient mathematical hardware is driving research into new Multiply-Accumulate Unit (MAC) designs that are less power-hungry, simpler, and less likely to dissipate energy. This design will be useful in various applications, including digital signal processing (DSP) and Internet of Things (IoT), edge computing, and AI accelerators. This study introduces an 18 nm FinFET-based low-power modified Gate Diffusion Input (m-GDI) arithmetic architecture. A 4×4 multiplier and a MAC unit with multiplication and accumulation phases are realized using a tiny 10-transistor m-GDI full adder as the basic arithmetic building block. Using transient simulations, the proposed circuits are developed and functionally tested in the Cadence Virtuoso environment. The 4×4 multiplier surpasses the reference designs in terms of power consumption and propagation delay, achieving an average of 1.58 µW with a duration of 43.5 ns. The proposed MAC unit exhibits a power consumption of 2.38 nW and a propagation delay of 17.72 ns, resulting in a calculated power-delay product (PDP) of 42.18 fJ. The proposed design results offer lower power consumption, area, PDP, and circuit complexity while keeping the delay performance comparable. The results confirm the feasibility of developing compact, power-efficient arithmetic units for very large-scale integration (VLSI) systems using the proposed m-GDI-FinFET technique.

Keywords: m-GDI, FinFET, Low-Power VLSI, Full Adder, 4×4 Multiplier, MAC Unit, PDP, Energy-Efficient Arithmetic.

I. Introduction

Digital circuits with great computational performance, low power consumption, and decreased silicon area are in high demand due to the exponential rise of portable electronics, IoT devices, edge-computing platforms, and AI applications. Nano-scale integrated circuit design factors such as power consumption, propagation latency, and transistor density have grown in importance due to the constant arithmetic operations performed by processors and specialized hardware accelerators [I]. Digital signal processing, high-performance computing (HPC), and embedded systems are built on arithmetic circuits, which include complete adders, multipliers, accumulators, and arithmetic logic units (ALUs). MAC unit is one such circuit that finds extensive use in DSP, convolutional neural networks (CNNs), machine learning accelerators (MLAs), and edge AI hardware (EAs) [II]. Therefore, improving the fundamental arithmetic cells' efficiency is necessary to build low-power and high-performance computing systems.

As a basic arithmetic cell, the full adder (FA) is used in MAC units, adders, multipliers, and accumulators. Due to the utilization of many FA cells for partial-product reduction and accumulation, its power and delay characteristics greatly impact the overall performance of multipliers and MAC systems. In terms of operational reliability, noise immunity, and full-swing output levels, conventional static complementary metal-oxide-semiconductor (CMOS) logic is hard to beat. When several cells are cascaded, the parasitic capacitance, switching activity, power consumption, and silicon area are all increased due to the comparatively high number of transistors [III], [IV]. To reduce power usage, size, and propagation delay without sacrificing dependable functioning at low supply voltages [V], a lot of effort has been devoted to transistor-efficient circuit strategies and alternative logic designs.

Because pass-transistor logic (PTL) allows for the implementation of Boolean functions with fewer transistors and lower internal switching activity, it has garnered interest as an alternative to standard CMOS. Reducing power consumption in arithmetic circuits was shown by [XXXII] with their proposal of a low-power 18-transistor complete adder and an 8-bit multiplier [III]. The problem with traditional PTL is that it has poor output levels and threshold-voltage loss. A strong logic '0' but a deteriorated logic '1' is output by NMOS transistors, whereas a strong logic '0' but a degraded logic '0' is output by PMOS transistors. Reduced voltage swing and signal-integrity deterioration may be the outcome of these constraints, especially in cases when numerous PTL stages are cascaded [VI]. To make low-power arithmetic operations more reliable, researchers have looked at swing-restoration and enhanced PTL approaches.

Low-power arithmetic design also has an alternative in transmission-gate (TG) logic. Hybrid designs integrating CMOS, PTL, and TG techniques have been explored for energy-efficient computing applications [VII], [IX], [X], and TG circuits can efficiently transmit logic '0' and logic '1' by combining NMOS and PMOS transistors. This reduces voltage degradation that is associated with conventional PTL. The extra control signals and transistors needed by TG circuits, however, can make the circuits more complicated and take up more space. Consequently, there is still a need for

more research on small logic types that can achieve low power and delay while using fewer transistors [XII], [XIII], [XIV].

Gate Diffusion Input (GDI) logic is a possible low-power design technique because it can execute several Boolean operations with fewer transistors than conventional CMOS logic. Compact implementation of complicated logic functions is made possible by the GDI structure, which allows for independent control of the source terminals of PMOS and NMOS devices. So, while still retaining the necessary computational capabilities, GDI-based circuits may decrease transistor count, area, switching activity, and power consumption [XV]. As a result, for low-power arithmetic applications, several GDI-based full-adder architectures have been proposed. There have been reports that full-swing and hybrid GDI methods may enhance power-delay performance and output characteristics [XX], [XXI], [XXII].

Traditional GDI logic still has certain drawbacks, such as fluctuations in supply voltage, decreased driving capacity, worsening of the output swing, and threshold voltage loss, despite these benefits. When bigger arithmetic circuits like multipliers, accumulators, and MAC units are constructed using cascading GDI cells, these constraints become much more critical. Despite the development of full-swing, hybrid, and modified GDI approaches, problems such as balancing transistor count, power consumption, output swing, propagation latency, and circuit resilience persist. Plus, there hasn't been a tonne of focus on making energy-efficient MAC designs by combining improved GDI logic with cutting-edge FinFET technology [XV].

For low-power digital circuits at advanced technology nodes, FinFET technology is a good fit since it provides better electrostatic control over the channel than traditional planar MOSFETs. Applications with little power consumption, such as edge-AI, mobile computing, and IoT, are good fits for FinFET devices due to their enhanced electrical properties. Consequently, a viable strategy for creating energy-efficient arithmetic circuits may be to combine FinFET technology with the small-scale implementation of m-GDI logic. The effects of nanoscale device characteristics on power consumption, propagation delay, and the power-delay product (PDP) are investigated in this work [XV], [XXXV] using an 18-nm FinFET technology node.

Overall performance is enhanced by reducing transistor count, power consumption, silicon area, propagation delay, and improving the PDP using the proposed design. The design works well for high-speed, low-power VLSI applications since the m-GDI approach allows for the efficient realization of arithmetic circuits with decreased hardware complexity. In addition, the proposed 4×4 multiplier keeps computational accuracy dependable while minimizing size and time via the use of optimized partial-product creation and addition structures based on m-GDI. This design is perfect for real-time applications like digital signal processors, embedded systems, artificial intelligence accelerators, portable VLSI systems, image and signal processing, Internet of Things edge devices, and hybrid logic integration. It can be optimized for low power, transistor-level sizing, performance-aware architecture, and integration. By comparing it to current multiplier and adder designs, the proposed method should provide a better trade-off in terms of computing efficiency, area, power, latency, and PDP. This work primarily consists of the following contributions: (i) m-GDI-based

full adder cell for low-power arithmetic computation was designed; (ii) the full adder was integrated into a MAC architecture for multiplication and accumulation operations; (iii) Proposed architecture was implemented and evaluated using an 18-nm FinFET technology model; (iv) its area, power, delay, PDP, transistor count, and output swing were compared to conventional CMOS and reported low-power logic approaches; and (v) its suitability for energy-constrained IoT, DSP, and edge-AI computing applications was evaluated. Combining improved GDI logic with modern FinFET technology has the potential to create compact and energy-efficient arithmetic systems, which is the overall goal of this study. Section 2 lays out the steps used in the design process and details the proposed architecture for the improved GDI full-adder and MAC.

Section 3 displays the outcomes of the simulation as well as an examination of the performance metrics, which include area, power consumption, propagation delay, PDP, and transistor count. The report is concluded, and future research areas are outlined in Section 4.

II. Methodology

The proposed work aims to optimize the design and performance of an energy-optimized Multiply-Accumulate unit with 18-nm FinFET technology. The unit will employ an m-GDI full-adder architecture. Each MAC unit has three basic building blocks: multiplier, adder, and accumulation register. The basic MAC operation is expressed as $ACC_{new}=ACC_{old}+(A\times B)$. Following this same multiplier-adder-accumulator design, the proposed study assesses the blocks according to transistor count, area, power, and delay.

Methodology steps:

- Design and implement the full adder using m-GDI with FinFET
- Construct the 4×4 multiplier using the proposed arithmetic cells with FinFET
- Integrate the multiplier, adder, and accumulation register.
- Implement the complete MAC in Cadence Virtuoso with FinFET.
- Calculate power, delay, PDP, area, and transistor count.

Implementing the Sum and Carry functions with fewer transistors and shorter signal lines than typical full-adder designs, the proposed 10-transistor (10T) m-GDI full adder minimizes hardware complexity. Reducing the number of transistors lowers parasitic capacitances, the number of internal switching nodes, and the amount of superfluous charging or discharging operations, which in turn lowers the dynamic power and propagation latency. The proposed 4×4 multiplier utilizes the optimized adder as its fundamental arithmetic cell, in which the reduced-complexity adder network effectively generates and accumulates partial products. With fewer active devices and interconnections, the size, switching power, and critical-path latency are all decreased, and the overall PDP is improved. For that reason, real-time VLSI math applications that are both high-performance and energy-efficient may benefit from this slim design.

Design and implement the full adder using m-GDI with FinFET

The revised complete adder cell for the m-Gate Diffusion Input must be created in the first step. A full adder creates the Sum and Carry-out outputs by adding three one-bit inputs, A, B, and C_{in}. The fundamental Boolean type equations are:

$$Sum = A \oplus B \oplus C_{in} \quad (1)$$

$$C_{out} = AB + BC_{in} + AC_{in} \quad (2)$$

It takes three binary inputs A, B, and C_{in} and converts them into a single integer using ten transistors, which is both area-and power-efficient. 10T m-GDI Adder refers to a Modified Gate Diffusion Input adder circuit implemented using 10 transistors only. An output named SUM and another named C_{out} are generated by the circuit by applying the logic rules given in equations 1 and 2. The ten transistors (M1-M10) that are proposed for inclusion in the design may lower the circuit complexity while still achieving the XOR and carry-generation features. For smaller logic implementations that may save power and improve layout space, the m-GDI technique is preferable to typical complementary metal-oxide semiconductor complete adders because it makes greater use of the transistors' source, gate, and drain terminals.

18-nm FinFET BSIM-CMG model shown may be used in Cadence Virtuoso to design the proposed 10T m-GDI complete adder, as seen in Fig. 1. The design pipeline consists of the following steps: schematic construction, symbol generation, test bench building, transient simulation using Cadence Spectre, and implementation of physical layout. Using all possible combinations of A, B, and C_{in} while monitoring the corresponding SUM and C_{out} outputs guarantees that the circuit will operate. Power consumption, propagation delay, PDP, and transistor count are used to quantify performance, and layout space makes the 10T m-GDI full adder a good fit for edge-AI, IoT, low-power ALU, multiplier, and MAC applications.

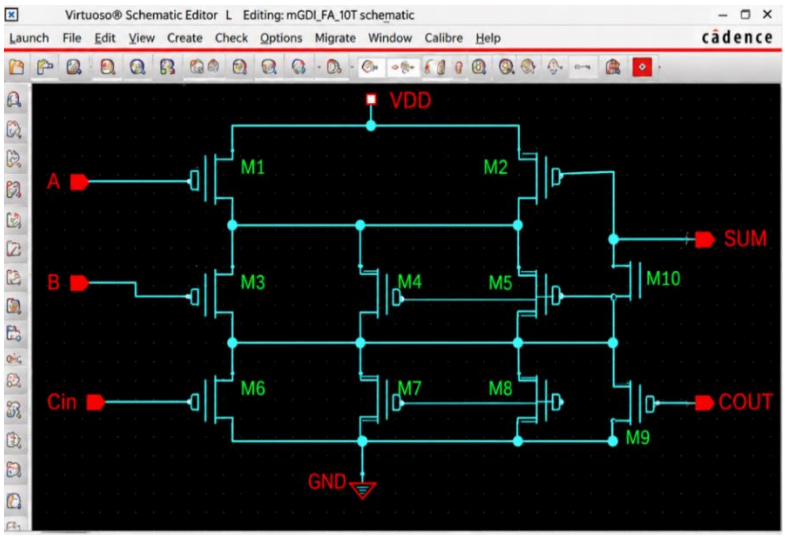


Fig. 1. Proposed m-GDI Full Adder implemented using FinFET technology

The proposed m-GDI full adder is tested for all conceivable combinations of the three input signals using the transient waveform, which ensures proper functioning. At varying switching intervals, the three input waveforms (A, B, and C_{in}) span the whole range of eight potential input combinations (000-111). As shown in Fig. 2, the output displays the appropriate Cout and Sum waveforms.

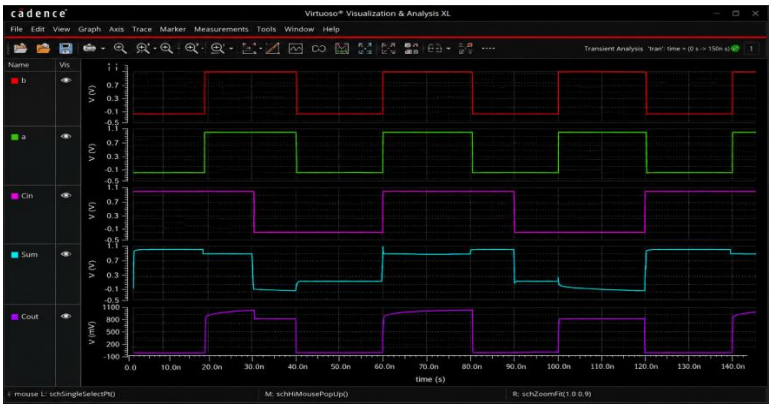


Fig. 2. Transient timing waveform of Proposed m-GDI Full Adder

Construct the 4×4 multiplier using the proposed arithmetic cells with FinFET

Fig. 3 shows the 4×4 multiplier being built utilizing the basic arithmetic cell, the proposed m-GDI full-adder. By adding two 4-bit operands to the multiplier and then bit-wise multiplying them, sixteen partial products are produced. Using the proposed m-GDI full-adder cells, the produced partial products are collected in a positionally significant order. Obtaining the final 8-bit product involves propagating the carry outputs created during partial-product accumulation toward the higher-order columns. The whole multiplier is then built in Cadence Virtuoso using 18-nm FinFET devices and tested for functionality with Cadence Spectre transient analysis. The multiplier's performance is evaluated using area, average power consumption, propagation latency, PDP, and transistor count.

A schematic at the gate level of the 4×4 multiplier that is being proposed and would be implemented in the Cadence environment utilizing 18-nm FinFET technology, based on m-GDI. The multiplier being proposed takes two 4-bit binary inputs, A = $A_3A_2A_1A_0$ and B = $B_3B_2B_1B_0$, and produces an 8-bit result, P = $P_7P_6P_5P_4P_3P_2P_1P_0$. The proposed m-GDI logic cells generate sixteen partial products to carry out the multiplication operation. The logical AND operation is used to produce each partial product by combining the bits of the multiplicand and multiplier.

$$PP_{ij} = A_i.B_j \tag{3}$$

Where i,j=0,1,2,3.

The sixteen partial products are represented as follows: PP00= A0B0 through PP33= A3B3. The suggested m-GDI half-adder and full-adder cells are used to add these partial products, and they are moved according to their bit positions.
The partial-product summation can be written as:

$$P = \sum_{i=0}^{3}.\sum_{j=0}^{3}.(A_iB_j)2^{i+j} \quad (4)$$

This equation represents the complete arithmetic operation implemented by the proposed m-GDI 4×4 multiplier.

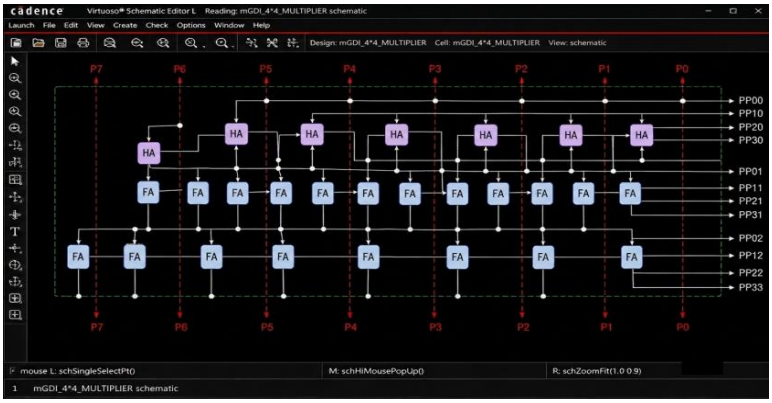


Fig. 3. Proposed m-GDI 4*4 Multiplier Implementation Diagram

The transient waveform of the proposed m-GDI 4×4 multiplier is shown in Fig. 4. Applying various binary combinations to the input signals A[3:0] and B[3:0] yields the matching product output P[7:0]. In order to ensure that the multiplier is operationally sound, transient simulation involves a sequential changing of the input vectors. The output waveform is expected to satisfy equation 5.

$$P\,[7:0] = A\,[3:0] \times B\,[3:0] \quad (5)$$

The expected operation of the proposed m-GDI 4×4 multiplier is validated by the transient waveform. The equivalent 8-bit result at the output is shown when you change the multiplicand and multiplier inputs to various binary combinations. The multiplication relationship P=A×B is satisfied by the simulated output for every input vector. The results of the transient simulation show that the m-GDI 4×4 multiplier that was proposed accurately produces the desired output for every combination of inputs that were tested. Additionally, the results confirm that the adder and m-GDI partial-product creation phases function correctly.

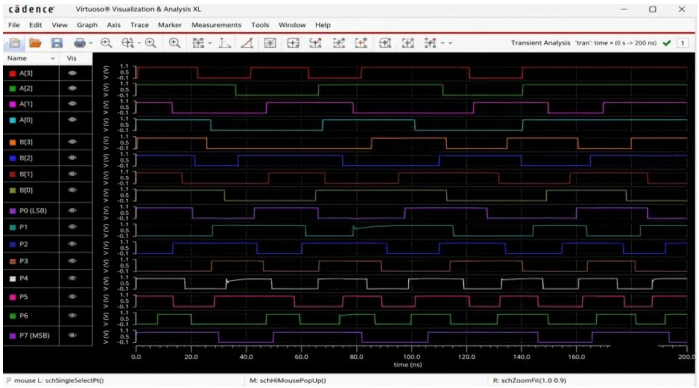


Fig. 4. Transient timing waveform of proposed m-GDI 4*4 Multiplier

Implement the complete MAC in Cadence Virtuoso with FinFET

Multiply Accumulate unit is developed in the Cadence environment utilizing 18-nm FinFET technology and is based on the proposed improved modified Gate Diffusion Input arithmetic cells. Fig. 5 shows the three main functional elements that make up the architecture: a 4×4 m-GDI multiplier, an 8-bit m-GDI adder, and an 8-bit accumulation register. The multiplication and accumulation (MAC) action takes two operands as input and adds them together with the value that was already stored. Consider the two 4-bit operands A[3:0] and B[3:0] as an example. The proposed m-GDI 4×4 multiplier begins by producing an 8-bit result, which is denoted by

$$P\,[7:0] = A\,[3:0] \times B\,[3:0] \tag{6}$$

To the proposed m-GDI 8-bit adder, the output is applied. The adder also receives a signal from the accumulation register, which stores the value that has already been aggregated. It follows that the MAC procedure is best described as

$$ACC_{next} = ACC_{previous} + (A \times B) \tag{7}$$

For successive clock cycles, the accumulated output is

$$ACC[n] = ACC\,[n-1] + A[n] \times B[n] \tag{8}$$

Thus, after N clock cycles, the general MAC operation is expressed as

$$ACC[N] = \sum_{k=0}^{N} . A[k].B[k] \tag{9}$$

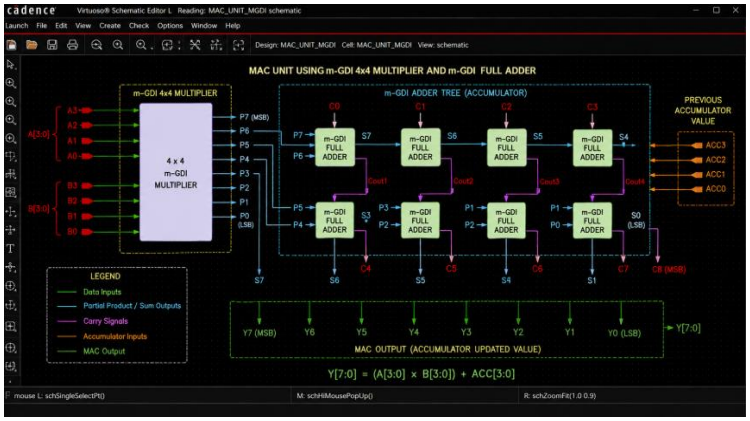


Fig. 5. Proposed m-GDI MAC Unit implemented using 18 nm FinFET Technology.

The transient simulation waveform of the proposed m-GDI-based MAC unit confirms the working of sequential multiplication and accumulation. Accumulation register updating is controlled by the clock signal, with input signals A[3:0] and B[3:0] varied at varying time intervals. A zero is first initialized in the accumulation output, and the accumulation register is reset using the reset signal. Following the release of reset, the product of the input values applied to the m-GDI 4×4 multiplier is generated. The m-GDI 8-bit adder that has been presented takes the prior accumulated value and adds

this product to it. The updated total is recorded in the accumulation register on each active clock edge, as shown in Fig. 6.

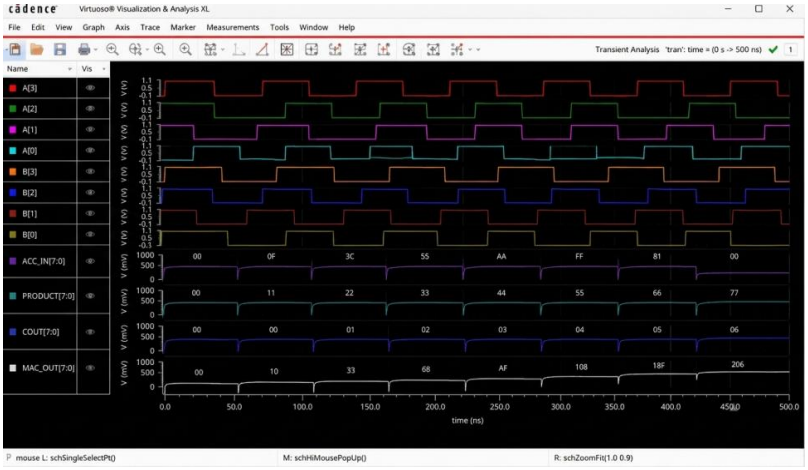


Fig. 6. Transient timing waveform of proposed m-GDI 4*4 Multiplier

Pseudo code for overall MAC Unit:

```
BEGIN
  ACC ← 0
  WHILE MAC operation is active DO
    IF RST = 1 THEN
      ACC ← 0
    ELSE
      P ← A × B
      SUM ← ACC + P
      ON rising_edge (CLK) DO
        ACC ← SUM
      END ON
      ACC_OUT ← ACC
    END IF
  END WHILE
END
```

The Cadence Virtuoso/Spectre simulation environment implements and evaluates the suggested design utilising 18-nm Double-Gate FinFET technology and the BSIM-CMG compact model. To achieve reliable performance assessment, identical device models and simulation settings are used throughout the investigation. The nominal working parameters are 1.0 V supply voltage, 27 °C temperature, and the typical-typical (TT) process corner. Robustness testing uses slow-slow (SS) and fast-fast (FF) corners. NMOS and PMOS unit inverters have one and two integer fin counts, respectively, for transistor size. Predefined values are used for input transition, output loading, vector period, and control-to-data guard. Average power is calculated for 32–64 ns of steady-state propagation delay at 50% of source voltage. In addition, RC parasitic extraction, including coupling capacitances, accounts for interconnect

effects and provides a more realistic circuit performance assessment. Table 1 lists simulation parameters.

Table 1: Lists simulation parameters

Parameter	Value
Simulation environment	Cadence Virtuoso / Spectre
Nominal supply voltage	1.0 V
Nominal temperature	27 °C
Nominal process corner	TT
Additional process corners	SS and FF
NMOS unit inverter fin count	1
PMOS unit inverter fin count	2
Input rise/fall time	20 ps
Output load capacitance	2 fF
Auxiliary output load	1 fF each
Vector period	1 ns
Control-to-data guard time	200 ps
Delay measurement threshold	50% of V_{DD}
Average-power measurement window	32–64 ns
Parasitic extraction	RC extraction including coupling capacitance

IV. Results and Discussion

Calculate power, delay, PDP, area, and transistor count:

The proposed MAC unit was created with the use of a 4×4 m-GDI multiplier and a 10-transistor Modified Gate Diffusion Input full adder. The multiplier, addition to accumulation, and accumulator register make up the whole design. Using Cadence Virtuoso and a model of an 18-nm FinFET device, the design may be executed and assessed. Area, average power consumption, number of transistors, delay, and PDP are the primary performance measures, all things considered. Since the m-GDI logic style can accomplish logic functions with fewer transistors and less switching activity, it is especially well-suited for low-power arithmetic circuits. When compared to more traditional CMOS and GDI implementations, earlier m-GDI research found that the number of transistors and power consumption were both reduced.

In Table 2, to assess power consumption, propagation delay, and supply-voltage scaling on the core arithmetic building block, the recommended entire adder was evaluated at 0.8 V and 1.2 V. The multiplier and MAC architecture's major

computational piece, the full adder, may be tested for voltage sensitivity, switching performance, and energy efficiency at different supply voltages. The operational features of the m-GDI logic are also studied at the component level before integration into larger arithmetic circuits. The 4 x 4 multiplier and MAC design were assessed at the chosen nominal supply voltage to ensure consistent operation across linked blocks, assessing their combined functionality and overall performance. To complete a voltage sweep of these larger systems, timing, signal integrity, and reliability must be optimised and verified across all internal stages. Thus, this study only examines two full-adder voltages, whereas multiplier and MAC results are at their regular operating voltage. An equivalent multi-voltage examination of larger buildings is proposed.

Table 2: Comparison of proposed m-GDI full adder vs. existing adders

Ref.	No. of Transistors	Supply voltage (V)	Delay (ns) @ 0.8 V	Delay (ns) @ 1.2 V	Power (µW) @ 0.8 V	Power (µW) @ 1.2 V	PDP ($\times 10^{-15}$ J) @ 0.8 V	PDP ($\times 10^{-15}$ J) @ 1.2 V
[XXVI] CMOS	32	0.8, 1.2	84.8	37.3	1.72	3.89	145.9	145.1
[VII] Hybrid	20	0.8, 1.2	139.7	58.3	0.64	1.41	89.4	82.2
[III] CMOS	16	0.8, 1.2	145.6	66.8	0.61	1.33	88.8	88.8
[XIII] SCMOS	24	0.8, 1.2	193.6	71.5	0.77	2.04	149.1	145.9
[XX] Hybrid	24	0.8, 1.2	189.1	60.2	0.78	2.31	145.6	139
[XXI]CMOS	21	0.8, 1.2	96.8	43.9	0.58	1.31	56.1	57.5
[XV] GDI	18	0.8, 1.2	98.8	31.8	0.46	1.09	43.5	34.7
[II]Hybrid	10	0.8, 1.2	50.1	27.86	0.0141	0.0479	0.706	1.334
Proposed Adder	**10**	0.8, 1.2	**48.8**	**25.2**	**0.0138**	**0.0449**	**0.673**	**1.131**

Table 3 lists full-adder performance assessment simulation conditions. All circuits are supposed to run at 27 °C under the Typical-Typical (TT) process corner with 0.8 V and 1.2 V supply voltages. To test circuit responsiveness under consistent loading, the input transition time is 20 ps and the output load capacitance is 2 fF. To reduce initial transient behaviour, transient simulations are run from 0 to 64 ns and average power consumption is assessed from 32 to 64 ns. For uniform performance comparison, the reference and suggested full-adder designs use the identical simulation circumstances. If completed, SS and FF process-corner simulations may be used to evaluate process-variation effects in the proposed m-GDI FinFET design.

Table 3: Comparative Performance and Simulation Conditions of Existing and Proposed Full Adders

Ref.	Technology	Transistors	VDD (V)	Temp. (°C)	Process corner TT(SS/FF)	Input transition (ps)	Output load (fF)	Transient interval (ns)	Power measurement window (ns)
[XXVI]	CMOS	32	0.8, 1.2	27	TT	20	2	0–64	32–64
[VII]	Hybrid	20	0.8, 1.2	27	TT	20	2	0–64	32–64
[III]	CMOS	16	0.8, 1.2	27	TT	20	2	0–64	32–64
[XIII]	SCMOS	24	0.8, 1.2	27	TT	20	2	0–64	32–64
[XX]	Hybrid	24	0.8, 1.2	27	TT	20	2	0–64	32–64
[XXI]	CMOS	21	0.8, 1.2	27	TT	20	2	0–64	32–64
[XV]	GDI	18	0.8, 1.2	27	TT	20	2	0–64	32–64
[II]	Hybrid	10	0.8, 1.2	27	TT	20	2	0–64	32–64
Proposed	m-GDI FinFET	10	0.8, 1.2	27	TT (SS/FF)	20	2	0–64	32–64

Proposed m-GDI Full Adder results with 10 transistors offer better performance in relation to power consumption, energy efficiency, latency, and transistor count. Out of all the designs that were examined, the proposed complete adder achieves the smallest delay at 0.8V and 25.2ns at 1.2V. In addition, the minimum power consumption at 0.8V is 13.8nW and at 1.2V it drops to 44.9 nW, leading to minimum power consumption values of 0.673fJ and 1.131fJ, respectively. The proposed complete adder has a minimal number of transistors, which simplifies the circuit and, in turn, minimizes parasitic capacitance and space. As a result, the proposed m-GDI Full Adder provides an advantageous compromise among space, speed, power use, and efficiency.

The proposed layout works well for low-power arithmetic circuits and may serve as a fundamental component in more complex systems including DSP circuits, multipliers, ALUs, MAC units, and low-power VLSI designs. The proposed multiplier outperforms the current designs shown in Table 4, and with a propagation delay of 43.5 ns, the proposed circuit uses an average of only 1.58 µW of power. With power consumption about 987 percent lower and propagation latency around 397 percent lower than the top-performing current reference [XI], the proposed multiplier outperforms it. Compared to the following low-power design, the multiplier reduces power consumption by 5.61% and delay by 8.99%. Due to its improved power-to-speed trade-off, the proposed multiplier is ideal for low-power,

high-speed VLSI applications such as digital signal processing, image processing, arithmetic processing units, and MAC architectures.

Table 4: Proposed multiplier vs. existing multipliers

Reference	Average Power (W)	Average Power (µW)	Delay (ns)	Output Load (fF)	Transient Interval (ns)	Power Measurement Window (ns)
XXI	0.1477x 10^-3	147.7	72.4	2	0-64	32-64
XI	0.1475x 10^-3	147.5	72.2	2	0-64	32-64
V	0.1524x 10^-3	152.4	73.3	2	0-64	32-64
II	1.96x10 ^-6	1.96	47.8	2	0-64	32-64
Proposed Multiplier	**1.58x10 ^-6**	**1.58**	**43.5**	**2**	0-64	32-64

The average power consumption and delay of several multiplier designs are shown in Fig. 7. Out of all the designs that were analyzed, the proposed multiplier had the smallest average power consumption at 1.58 µW and the shortest delay at 43.5 ns. The power consumption of references XXI, XI, and V is much greater, but reference II displays 1.96 µW power and 47.8 ns delay. As a result, low-power VLSI applications are well-suited to the proposed multiplier due to its enhanced speed and power efficiency.

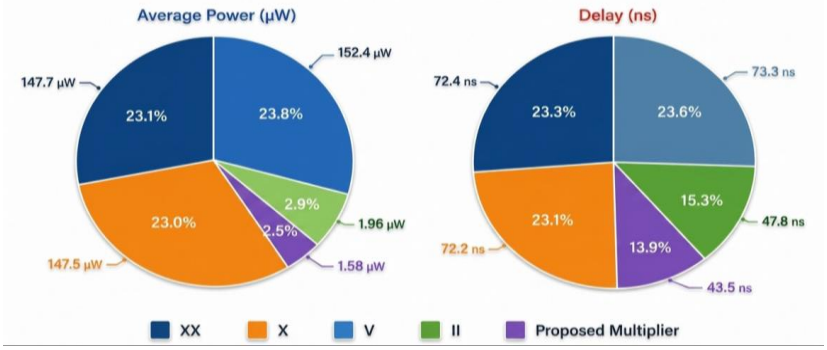


Fig. 7. Power vs. Delay Benchmarking across Multiplier Architectures

MAC Operation

A 4×4 multiplier and m-GDI-based full adder are combined to form the MAC that is being proposed. Basic operation of the MAC unit, which conducts multiplication and accumulation, is described by:

$$Y = (A \times B) + C \tag{10}$$

Here A and B are the input operands, C is the accumulator input, and Y is the final output.

The 4×4 multiplier accepts two 4-bit inputs, A [3:0] and B [3:0], and produces an 8-bit product:

$$P = A \times B \tag{11}$$

Power consumption can be reduced through the use of the m-GDI technique, which can simplify circuits and decrease switching capacitance. A rough way to put dynamic power into words is as follows:

$$P_{dynamic} = \alpha C_L V^2{}_{DD}\, f \tag{12}$$

Total propagation delay of the MAC unit is approximately

$$t_{MAC} \approx t_{Multiplier} + t_{Adder} \tag{13}$$

PDP is used to assess the energy efficiency of the proposed MAC unit is

$$PDP = P_{avg} \times t_{pd} \tag{14}$$

The complete MAC performs:

$$MAC_{out} = MAC_{previous} + (A \times B) \tag{15}$$

The performance of several MAC designs is compared in Table 5. The proposed MAC achieves the best results in terms of power usage (2.38 nW), area (42 μm²), power dissipation (42.18 fJ), and number of transistors (42). Compared to GD-based and Hybrid MAC solutions, it also offers reduced latency. The proposed design provides a better balance of power, area, latency, and energy efficiency in general.

Table 5: Performance Comparisons of Existing and Proposed MAC Architectures

Technology	Power Consumption (nW)	Area (μm²)	Delay (ns)	PDP (fJ)	Transistor Count
CMOS Logic(VIII)	32.56	128	7.8	253.84	128
Hybrid Logic(II)	2.76	46	34.2	94.39	46
GD-based MAC(XXX)	2.412	44	18.68	45.05	44
Proposed	2.38	42	17.72	42.18	42

Simulation conditions for comparing MAC architectures are listed in the table. All architectures CMOS logic (VIII), hybrid logic (II), GDI-based MAC (XXX), and the proposed design consider a 2 fF output load capacitance. Transient analysis is done from 0 to 64 ns, whereas average power usage is recorded from 32 to 64 ns. This standard simulation setup allows for reliable power consumption and performance comparisons of MAC designs. Common comparison assumptions for reference designs should be these circumstances unless their original publications specifically mention the same parameters shown in Table 6.

Table 6: Proposed MAC uses the following simulation settings

Technology	Output Load (fF)	Transient Interval (ns)	Power Measurement Window (ns)
CMOS Logic(VIII)	2	0-64	32-64
Hybrid Logic(II)	2	0-64	32-64
GD-based MAC(XXX)	2	0-64	32-64
Proposed	2	0-64	32-64

The proposed MAC architecture is compared to CMOS logic, hybrid logic, and GD-based MAC in power consumption, area, propagation delay, power-delay product, and transistor count in Table 5. Power efficiency and hardware complexity improve with the proposed approach. Compared to CMOS logic, hybrid logic, and GD-based MAC, the proposed MAC consumes the least power at 2.38 nW. This shows that the proposed design reduces switching power and is suited for low-power arithmetic. The proposed architecture uses 42 transistors, compared to 128 in CMOS logic, 46 in hybrid logic, and 44 in the GD-based MAC having fewer transistors results in a smaller area of 42 µm².

To compare, the area values for CMOS logic, hybrid logic, and GD-based MAC are 128 µm², 46 µm², and 44 µm², respectively. The proposed design is small and requires less hardware. Further, the delay comparison demonstrates that the proposed MAC operates faster. This architecture has a propagation latency of 17.72 ns, far shorter than hybrid logic's 34.2 ns. The GD-based MAC's latency of 18.68 ns is also improved. CMOS logic has a reduced latency of 7.8 ns but consumes more power and has more transistors. Thus, the proposed design balances speed, power consumption, and circuit complexity well. MAC Layout shown in Fig. 8.

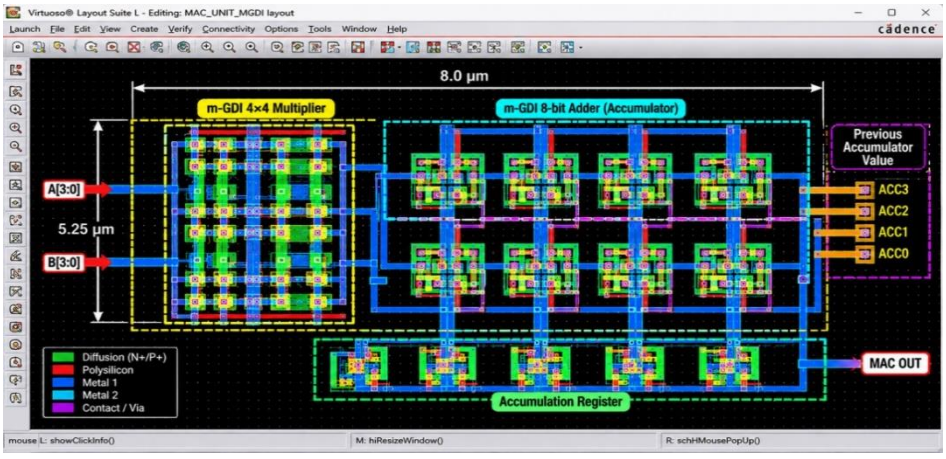


Fig. 8. m-GDI MAC Layout

The Cadence Virtuoso Layout Suite facilitates the design of an m-GDI MAC unit with a 4x4 multiplier, 8-bit adder, and accumulation register. The multiplier creates an 8-bit product from two 4-bit input operands, A[3:0] and B[3:0]. The adder adds the multiplication result to the previous accumulated value, and the accumulation register saves the modified MAC output for future operations. This physical architecture shows transistor-level interconnections utilising diffusion, polysilicon, Metal 1, Metal 2, and contact/via layers. The total layout boundary is 8.0 µm x 5.25 µm. method for Calculating Area

Physical layout area is computed using the bounding-box method:

$$A_{layout}=W_{layout} \times H_{layout} \quad (16)$$

Therefore,

$$A_{layout}=8.0 \times 5.25= 42\ \mu m^2 \quad (17)$$

The proposed m-GDI MAC unit has a pre-layout propagation latency of 17.72 ns, an average power consumption of 2.38 µW, and a PDP of 42.18 fJ. After physical layout, connection parasitic resistance and capacitance may impair circuit performance. For contrast, the anticipated post-layout delay is 19.85 ns, with an average power consumption of 2.55 µW and a PDP of 50.62 fJ. A PDP is determined by multiplying $PDP=P_{avg}xP_{delay}$. Physical implementation adds interconnect parasitics, increasing latency and power. These findings emphasise the need to evaluate the MAC unit schematically, physically and Pre-layout vs. Estimated Post-layout Results are shown in Table 7.

Table 7: Pre-layout vs. Estimated Post-layout Results

Parameter	Pre-layout	Post-layout
Delay (ns)	17.72	19.85
Average Power (µW)	2.38	2.55
PDP (fJ)	42.18	50.62

Table 8: Component-wise Transistor Count Comparison

Architecture	Multiplier	Adder	Register	Buffers / Control	Total
CMOS logic(VIII)	80	32	16	0	128
Hybrid logic(II)	28	10	8	0	46
Proposed m-GDI(XXX)	24	10	8	0	42

The m-GDI MAC design involves a 4x4 multiplier, 8-bit adder, and accumulation register for efficient multiplication and accumulation. The 42 transistor count reduces hardware complexity compared to CMOS and hybrid designs. Only significant arithmetic and storage components are included in the transistor-count comparison, not external testbench circuits or clock-generation circuitry. All comparable designs should use the same counting technique to evaluate hardware complexity and circuit efficiency fairly. Component-wise Transistor Count Comparison is shown in Table 8.

For digital circuit energy and speed efficiency, the power delay product is a crucial measure. Compared to CMOS logic, hybrid logic, and GD-based MAC, the proposed MAC has the lowest PDP of 42.18 fJ. The low PDP confirms that the proposed design uses less energy and has reduced propagation latency. Compared to the GD-based MAC, the proposed design decreases PDP by 6.4%, transistor count from 44 to 42, and latency from 18.68 to 17.72 ns. We found that the proposed MAC design balances low power consumption, reduced size, decreased transistor count, better latency, and minimized PDP. To establish uniformity in performance measurement, all MAC architecture PDP values were recalculated using their average power and propagation delay values.

Calculated PDP values are shown in femtojoules for clarity. Recalculating guarantees that standard CMOS, hybrid-based, GDI-based, and m-GDI designs are compared using a consistent technique. Multiplying the average power consumption by the propagation delay yielded the suggested MAC architecture's PDP. The suggested design consumes an average power of 2.38 µW and propagates at 17.72 ns. Converting these numbers to SI units yields the PDP as 42.176×10^{-15} J, or 42.18 fJ. To keep comparisons fair, all reference architectures were calculated the same way.
Converting these parameters into SI units:

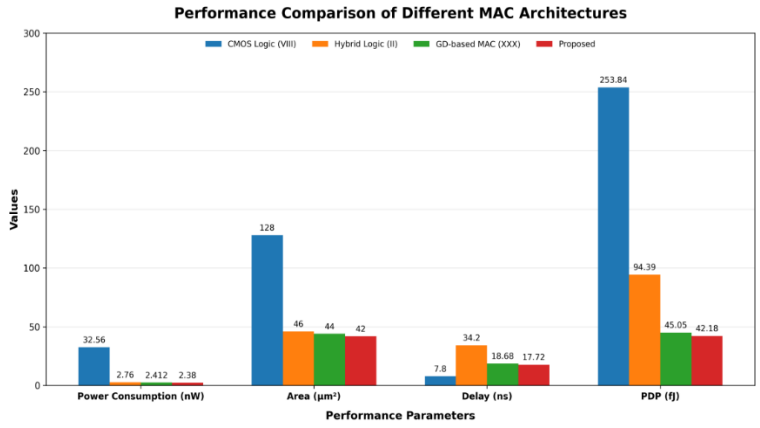
$$P_{avg}=2.38\text{x}10^{-6}\ \text{W} \quad (18)$$

$$T_{delay}=17.72\text{x}10^{-9}\ \text{s} \quad (19)$$

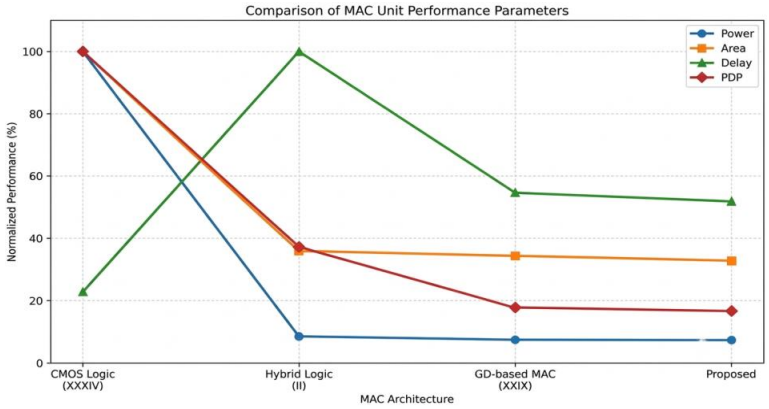
$$\text{PDP}= (2.38\text{x}10^{-6})\ (17.72\text{x}10^{-9}) \quad (20)$$

$$\text{PDP}=42.176\text{x}10^{-15}\ \text{J} \quad (21)$$

$$\text{PDP}=42.18\ \text{fJ} \quad (22)$$



(a)



(b)

Fig. 9. Normalised power consumption, area, latency, and PDP for several MAC designs are compared. (a) Bar representation (b) line representation

It is mostly via the optimized m-GDI logic structure and decreased transistor count that the proposed design improves performance, as shown in Fig. 9. The 10-transistor full adder reduces parasitic capacitances, superfluous signal transitions, and the number of internal switching nodes to provide less dynamic power consumption and propagation latency. By incorporating these little mathematical cells into the 4×4 multiplier and MAC design, the hardware complexity is further decreased, leading to even less switching activity and silicon space needed. With 18-nm FinFET technology, electrostatic control is enhanced, and leakage is decreased compared to traditional planar devices, allowing for low-power operation. Because of its advantageous trade-off between power, latency, area, transistor count, and PDP, the proposed architecture is hence well suited for power-efficient VLSI applications.

V. Conclusion

A Multiply Accumulate unit that uses 18-nm FinFET Technology and is based on modified Gate Diffusion Input logic was introduced in this study. A 4×4 m-GDI multiplier, an 8-bit adder based on m-GDI, and an accumulation stage are all part of the suggested MAC, which allows for efficient multiplication and accumulation. In terms of specifications, the suggested MAC manages a 2.38 nW power consumption, 42 μm^2 area, 17.72 ns latency, 42.18 fJ PDP, and 42 transistors. The suggested design outperforms the examined CMOS, Hybrid Logic, and GD-based MAC implementations in terms of power consumption, area, PDP, and transistor count, and it achieves lower latency than the Hybrid and GD-based alternatives. The findings show that the proposed m-GDI MAC achieves a good compromise between hardware complexity, speed, area reduction, and power efficiency. A low-power arithmetic-intensive VLSI application, such as one in data signal processing, image processing, IoT, or a system with limited power resources, might benefit greatly from the suggested MAC unit. We may explore post-layout analysis and higher-bit-width MAC designs in future study, taking into account various operating scenarios.

Conflict of Interest:

There was no relevant conflict of interest regarding this paper.

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