JOURNAL OF MECHANICS OF CONTINUA AND MATHEMATICAL SCIENCES
www.journalimcms.org

ISSN (Online) : 2454 -7190 Vol.-21, No.-07, July (2026) pp 1-18 ISSN (Print) 0973-8975

A CONCEPTUAL FRAMEWORK FOR THE DEVELOPMENT OF A CYBER-PHYSICAL TEST BENCH FOR PRINTED CIRCUIT BOARD ASSEMBLY PRODUCTION

Andre Fred Du Plooy[1], Arthur James Swart[2], Pierre Eduard Hertzog[3]

[1,2,3] Department of Electrical, Electronic and Computer Engineering, Central University of Technology, Bloemfontein, Free State, South Africa.

Email: duplooyandre834@gmail.com, aswart@cut.ac.za, phertzog@cut.ac.za

Corresponding Author: **Andre Fred Du Plooy**

https://doi.org/10.26782/jmcms.2026.07.00001

(Received: April 09, 2026; Revised: July 01, 2026; Accepted: July 12, 2026)

Abstract

Printed Circuit Board Assembly (PCBA) testing continues to represent a key, but relatively expensive, phase in electronics manufacturing, particularly in high-mix, low-volume production environments for small- to medium-sized enterprises (SMEs). In response to growing product complexity and variability in manufacturing quality, test benches are pivotal in delivering good quality, reliability, and regulatory compliance. Although Industry 4.0 drives smart manufacturing through IoT, modular engineering, and data-driven optimization, the existing architecture of academic and industrial PCBA test benches remains fragmented. Automation, connectivity, and analytics are frequently implemented as stand-alone solutions rather than as components of an integrated, cohesive framework. This study presents a conceptual framework for the development of a cyber-physical PCBA test bench, combining modular hardware, in-house manufacturing, IoT-enabled data acquisition, and AI-based analytics in a unified, scalable architecture. Based exclusively on established literature, the framework condenses literature on past IoT implementations, modular test-bench analyses, cost-cutting techniques, and software-centric optimization perspectives associated with SME manufacturing contexts. The framework highlights the shortcomings in scalability, cost efficiency, interoperability, and analytical capability that are identified in the literature by conceptualizing the test bench as a responsive, data-oriented aspect of the larger manufacturing ecosystem. As a conceptual contribution, the framework provides groundwork for future empirical validation and industrial application by moving away from static, deterministic testing structures and towards smart, cyber-physical quality assurance systems grounded in Industry 4.0.

Keywords: PCBA testing, Industry 4.0, modular test bench, IoT integration, AI-driven optimization

I. Introduction

Production systems, especially those that are rigid and inflexible according to product requirements and operational uncertainty, make it difficult to maintain consistent product standards [V], [VI]. Underpinning this growing complexity of quality assurance within the current electronics manufacturing context, we see a significant and increasing functional density, tighter tolerances, and shorter product lifecycles all posing challenges to production testing infrastructure [VI], [XXIX]. The increasing complexity of Printed Circuit Board Assemblies (PCBAs), together with accelerated product development cycles, places significant strain on traditional test-bench infrastructures. These benches typically rely on fixed instrumentation, externally sourced fixtures, and siloed data repositories, which collectively limit their ability to meet Industry 4.0 requirements for flexibility, traceability, and real-time optimization.

Modern studies increasingly show that smart testing environments that include not only IoT connectivity, but also digital traceability and data-driven decision-making through manufacturing and quality-assurance processes, are urgently needed [VI], [XXIX]. Such integration in theory provides real-time visibility, predictive diagnostics, and closed-loop optimization. In reality, however, existing PCBA test-bench solutions generally tend to tackle all of these dimensions in isolation. Modular fixtures may be implemented without the analytical or data integration capabilities required, and IoT connectivity is often implemented as part of legacy systems without architectural coherence or semantic alignment [XX], [XIV]. Consequently, many test benches are functionally automated but analytically passive and do not contribute to long-term process improvement.

This fragmentation is particularly troublesome for a small-to-medium enterprise (SME) with acute cost constraints, varying product portfolios, and limited ability to undertake large-scale investment in infrastructure. History of IoT deployments shows that without the proper architectural orientation, advanced digital technologies such as IoT may increase complexity instead of providing observable operational benefit [XIV], [XXX]. As a result of that, there is an increasing demand for test-bench architectures that are technologically advanced, economically viable, modular, and scalable in SME manufacturing environments.

This study aims to solve the research problem of an insufficient cohesive conceptual framework that can tie together all four relevant aspects of modern PCBA testing:

1. A modular test-bench based architecture allows the reconfiguration of hardware and software between different product variants.
2. Internet of Things (IoT) to enable data integration, interoperable communications and structured data acquisition.
3. Cost reduction and the opportunity for in-house manufacturing, focusing on fixtures and test interfaces.
4. AI-based test optimization, using historical data for predictive diagnostics and ongoing improvement.

As such, this study proposes a conceptual framework for an in-house-manufactured, cyber-physical, modular PCBA test bench that is compliant with Industry 4.0 principles and designed for use in SME enterprise manufacturing environments. Section 2 reviews

current academic test-bench architectures with specific emphasis on modularity, automation, and scalability. It further examines their structural limitations, thereby establishing the need for a more cohesive and integrated solution. Section 3 extracts lessons learned from past IoT applications in manufacturing to provide a more comprehensive perspective on how to tackle cost, interoperability, and legacy system constraints in an SME context. In Section 4, cost-reduction mechanisms in test-bench engineering are discussed with modularization, fixture reuse, and in-house manufacturing as primary drivers of capital and operational cost reduction. Section 5 presents an AI-centric solution towards an optimization strategy, with QR-based identification, software-defined debugging, modular test scripting, structured data storage, etc., enabling higher-order analysis and predictive capabilities. Section 6 draws together these dimensions into the overall conceptual framework of integrating IoT with the test bench by defining the interaction of cyber-physical elements, data systems, and networks. Section 7 summarizes the proposed framework, describing its limitations, and laying the groundwork for future empirical validation and industrial implementation.

II. Analysis of Existing Test-Bench Architectures

Recent academic paradigms reveal incremental advances towards automation and modularity around PCBA testing, yet most remain limited to partial integration of the systems under discussion, as they are still not fully aligned with the flexibility and scalability requirements of Industry 4.0 fabrication. Balaji et al. [II] introduce an automatic PCBA diagnostic framework including software-controlled instrumentation, pogo-pin fixtures, and machine learning-based fault tagging. The system achieves repeatable measurements, structured data logging, and automated diagnostic capability. However, the framework is still heavily dependent on laboratory-grade commercial off-the-shelf (COTS) instruments and fixed fixture layout, which restricts cost efficiency, flexibility, and scalability—particularly in SME production environments requiring tightly controlled capex.

A similar pattern can be detected in Shah et al [XXII], who develop a compact automated test bench for portable measurement devices via a state-machine-driven software development framework and internal loop-back testing. Though this method effectively minimizes the number of external instrumentation and shortens operational flow, it is intrinsically product-specific and does not scale easily to heterogeneous PCBA families that differ in electrical interfaces, power requirements, and functional domain. In this scenario, the architecture does not have the generality that high-mix manufacturing applications could need.

Larger studies emphasize these limitations. Nkadimeng et al. [XIX] present a modular and automated test bench of ATLAS low-voltage power supplies. It results in significant reductions in test time and duplication across the program thanks to interchangeable interface boards and the reuse of software. The system is designed for large-scale scientific instrumentation environments and depends on specialized infrastructure that is not accessible to SMEs. Likewise, Dello Sterpaio et al. [VII] propose a PXI-based electronic ground support equipment (EGSE) framework allowing sophisticated protocol-level diagnostics but rely on expensive instrumentation ecosystems that restrict functionality outside niche domains.

Taken together, these studies show that partial modularity could be achieved at the software and interface level; however, full modularity to include fixtures, measurement subsystems, and debug tooling is also an emerging challenge. Hardware reusability is also poor; fixtures are not easily reconfigured, and technician-focused diagnostic workflows are underdeveloped. The inherent limitations necessitate a test-bench design that is entirely modular, reconfigurable, and in-house produced, allowing for a variety of PCBA products to reach cost-bound manufacturing systems.

III. Lessons from Historical IoT Implementations

A study in the past, as evidenced by previous research on Industrial IoT implementations in the manufacturing sector, identified architectural and scalability limitations with existing test-bench designs as typical challenges [XIV], [VI], [XX]. Previous research consistently discovers three intertwined barriers to effective IoT adoption: cost, interoperability, and legacy-system integration [XXX], [I], [XX].

From a financial viewpoint, Yang et al. [XXX] highlight that SMEs commonly face prohibitive upfront investment costs and uncertain return on investment when adopting IoT systems. Such fears are even more acute when benefits are achieved only after long periods of operation. In agreement with this perspective, Babu et al. [I] also pointed out that hidden costs—specifically with regard to device heterogeneity, middleware development, and maintenance—each contribute to reducing the perceived economic viability of IoT adoption in an industrial setting.

Interoperability is still one of the longstanding technological barriers. Onu et al. [XX] note that the lack of standard protocols used for communication and the high proliferation of legacy devices with no digital interfaces are key obstacles to IoT deployment in industries, particularly in developing countries. The present results are consistent with the findings of Industry 4.0 synthesis of Chen et al. [VI], which highlights that these disjointed communication stacks hamper real-time data streaming, system coordination, and closed-loop optimization.

Furthermore, Lee et al. [XIV] show that legacy hardware cannot easily and rapidly blend into a cyber-physical manufacturing architecture and fails to be integrated as part of a digital control loop in general without extensive retrofitting. Combined, these findings demonstrate that the addition of IoT to PCBA test benches must prioritize architectural simplicity, backward compatibility, and streamlined communication protocols. The framework that is proposed in this study explicitly incorporates these principles to provide a practical model for SME manufacturing practices.

IV. Cost-Reduction Strategies in Test-Bench Engineering

Cost is the primary constraint throughout past and recent IoT deployments and literature in test-bench engineering applied to SME manufacturers due to their capital expenditure constraints. Fiedler et al. [VIII] consider jigs and fixtures to be 10–20 % of overall manufacturing system cost; they seem to be strategic leverage points for cost optimization in PCBA testing situations.

Empirical evidence suggests that organized redesign methodologies can have significant financial and operational benefits. Kibbe et al. [X] found a considerable per-test cost reduction through the Design-for-Six-Sigma-based redesign of fixtures that

can also lead to yield and operational reliability improvements. In high-performance electronics testing settings, Nkadimeng et al. [XIX] also prove that modular test benches reduce redundancy, calibration challenges, and lifecycle cost by utilizing hardware/software reuse and standardization.

On a systems level, Brecher et al. [IV] state that modular production and testing platforms allow lifecycle cost reduction by reuse, simplified calibration, and distributed replication. Supporting this, Moayedi [XVI] showed how standardized modular test infrastructures implemented at a variety of institutions lead to considerable reductions in logistical and operational expenses, while remaining consistent in measurements.

Notwithstanding this amount of evidence, there are few or no existing studies, according to the author's knowledge, where an empirical study explicitly measures the advantages of PCBA test benches manufactured in-house for an SME context. Such a gap directly motivates the framework proposed in this study, where internal fixture fabrication, modular hardware re-use, and additive manufacturing are treated as core mechanisms used to reduce both capital and operational expenditure.

To avoid treating in-house manufacturing as an assumed economic advantage, the proposed framework incorporates a lifecycle-cost model for evaluating SME feasibility [XXV]. The model compares the total cost of ownership of an in-house modular test-bench approach with a commercially supplied modular test system. This follows lifecycle-costing principles, where capital, operating, maintenance, downtime, and replacement costs are evaluated over the useful life of the asset rather than only at the purchase stage [XII] [IX].

The lifecycle cost of the in-house test-bench option is expressed as:

$$LCCIH = Cdesign + Cequip + Cfab + Cmat + Clab + Ccal + Cmaint + Csoft + Cdown + Ctrain - S$$

where Cdesign is the engineering design cost, Cequip is the amortised cost of internal fabrication equipment, Cfab is additive or subtractive fixture fabrication cost, Cmat is material cost, Clab is assembly and engineering labour, Ccal is calibration cost, Cmaint is maintenance cost, Csoft is test-software development and database-integration cost, Cdown is downtime or production-loss cost, Ctrain is operator and technician training cost, and S is residual or reuse value of fixtures, modules, and equipment.

The lifecycle cost of the commercial alternative is expressed as:

$$LCCCOM = Cpurchase + Cvendor + Clic + Ccal\text{-}v + Cmaint\text{-}v + Ccustom + Cchange + Cdown + Cdep - Scom$$

where Cpurchase is the capital purchase cost of the commercial system, Cvendor is supplier integration cost, Clic is software or support licensing, Ccal-v is vendor calibration cost, Cmaint-v is vendor maintenance cost, Ccustom is customization cost for product-specific fixtures, Cchange is product-change or fixture-redesign cost, Cdown is downtime cost, Cdep is depreciation, and Scom is residual value. The economic feasibility condition is therefore:

$$LCCIH \leq LCCCOM$$

For production planning, the cost per tested unit may be expressed as:

$$CPU = LCC / NT$$

where N is the number of units tested per year, and T is the useful life of the test-bench system in years. The break-even production volume is reached when the difference in fixed cost between the in-house and commercial options is offset by lower fixture-reuse, customization, maintenance, and product-change costs [III]. This may be expressed as:

$$NBE = (FIH - FCOM) / (VCOM - VIH)$$

where NBE is the break-even volume, FIH and FCOM are the fixed costs of the in-house and commercial alternatives, and VIH and VCOM are the respective variable costs per tested unit.

Sensitivity analysis is applied by varying the main SME cost drivers: annual production volume, number of PCBA variants, fixture-reuse percentage, engineering labour rate, additive-manufacturing cost, calibration frequency, downtime cost, and product-change frequency [XXXI]. Three scenarios are proposed. A low-volume/low-variation scenario may favour commercial systems where internal design cost cannot be absorbed over sufficient output. A medium-volume/high-variation scenario may favour modular in-house fixtures because design reuse and lower customization cost become more significant. A high-volume/high-variation scenario is expected to provide the strongest case for in-house manufacturing, provided that calibration control, engineering support, and fixture reliability are maintained.

The model therefore does not claim that in-house manufacturing is always cheaper. Rather, it defines the conditions under which the claim can be evaluated. In-house fixture development becomes economically favourable only when lifecycle savings from reuse, rapid redesign, local maintenance, and reduced supplier dependency exceed the additional internal costs of engineering, calibration, training, and fabrication infrastructure. This makes the proposed framework suitable for SME feasibility assessment because it links the technical architecture to measurable economic variables rather than relying only on qualitative cost-reduction arguments.

V. AI-Centric Optimization Strategy for PCBA Test Benches

Modular design and in-house manufacturing solve structural cost drivers within PCBA lines, but longer-term optimization increasingly requires intelligent, data-centric methods. As demonstrated by Schuitemaker and Xu [XXI] and through empirical evaluations of Industry 4.0 case studies by Narula et al. [XVII], QR-code-based identification allows for unit-level traceability and structured data collection between construction and test stages. This manner allows a direct connection between individual PCBA units and test histories in full.

The data integrity and the auditability can be additionally enriched with distributed ledger technologies. Wang et al. [XXVIII] also show how blockchain-enabled traceability increases the trust of data and the resistance of data-to-data tampering, whereas Li et al. [XV] generalize this to complex assembly workflows by hierarchical indexing methods that are relevant to PCBA work.

Software debugging is an essential enabler for optimization. Balaji et al. [II] and Shah et al. [XXII] demonstrate that modular software architectures permit selective test execution and targeted fault isolation without requiring physical reconfiguration, which is known as selective fault isolation. Siddiqui et al. [XXIV] and Verani et al. [XXVII] extend these capabilities and demonstrate that software-centric diagnostics reduce test iteration time and increase yields in industrial electronics testing.

At a higher analytical level, predictive modelling and machine learning-based defect classification enable the optimization of dynamic testing scenarios. Stoyanov et al. [XXVI] and Siddiqui et al. [XXIII] show that historical test data could help in reducing the number of tests, setting limits of acceptance, and making diagnostics faster. The integration of modular test scripts, structured SQL databases, and analytics is taken as the analytical backbone for the proposed framework and is based on Python.

VI. Conceptual Framework for IoT-Enabled Test-Bench Integration

Combining modular hardware concepts, cost-reduction pathways, and AI-powered optimization methods discussed above can enable a unified cyber-physical architecture that can facilitate interoperable data exchange, system cohesion, and long-range scalability. Prior research in cyber-physical manufacturing systems stresses that the integration of devices is not possible by simply adopting one new technology, but rather, by implementing a layered architecture where physical assets, communication protocols, data models, and analytics perform cohesively as well [XIV], [VI].

This conceptual framework integrates all these requirements into a complete cyber-physical test-bench architecture that is consistent with Industry 4.0 principles. At its foundation, modular hardware components interface with PCBA units through reconfigurable in-house-manufactured fixtures. The design response in this manner directly targets cost and scalability constraints revealed in the historical test-bench and IoT implementations, which were characterized by fixed fixtures and outsourced tooling that reduced adaptability and increased lifecycle cost [VIII], [XIX]. Inside each test module are embedded controllers serving measurements and controls that are only needed in localized and deterministic execution, reducing dependence on laboratory-grade instrumentation for the larger datasets within these units.

At the connectivity level, the framework supports communication mechanisms based on lightweight and interoperable protocols for embedding hardware heterogeneity. Measurement results, status events, and control signals generated by embedded controllers are transmitted using the industrial IoT protocols MQTT and OPC UA. These protocols align with established implementation strategies for scalable and interoperable Industrial IoT deployments [XX], [XIII]. OPC UA provides semantic information modelling and links with the ISA-95 automation hierarchy through structured integration between low-level devices and higher-tier ones like Manufacturing Execution Systems (MES) or quality systems [XIII]. Concurrently, MQTT also provides low-overhead publish–subscribe communication for resource-constrained embedded devices, in which cost and performance can be handled from a cost and performance perspective, as proposed in earlier SME IoT research papers [I], [XXX].

The data layer is the middle layer, a layer above the connectivity layer, and provides the backbone for the cyber-physical architecture. Results from tests are maintained in SQL databases and indexed with QR-code-based unit identifiers to allow traceability at the unit level during testing, rework, and deployment stages as well [XXI], [XVII]. At the top level, each stored record incorporates metadata such as firmware revisions, test phases, operator identifiers, and environmental conditions. This structured enrichment reflects data-driven manufacturing constructs aligned with Internet of Production paradigms proposed by Brecher et al. [V]. This step-by-step method guarantees that both isolated events (think pass/fail and resetting) and continuous measurements (such as voltage, current, or timing profile measurements) can be queried and analysed efficiently in large production databases [V], [XVIII].

At the intelligence layer, AI-based analytics works atop this data backbone, turning the test bench from a deterministic validation centre to a learning system that is capable of predictive diagnostics and continuous optimization. Machine learning-based analysis of historical test data is showing promising results in the field of electronics manufacturing, allowing to predict early failure, optimizing limits in the light of test data according to adaptive limits [XXVI], [XXIII], [XXIV]. Through integration of such analytic powers into the test-bench model, cyber-level analysis-based knowledge can be utilized to directly contribute to test execution strategies, debugging steps, and fixture design iterations.

As illustrated in Figure 1, the proposed cyber-physical test-bench architecture is a layered test-bench architecture consistent with Industry 4.0 and the ISA-95 automation hierarchy [XIII]. At the physical level, modular and in-house-manufactured fixtures are used to provide scalable and cost-effective electrical access to PCBA units — it can be used in high-mix/low-volume SME production environments. At the connectivity layer, abstraction of device-level diversity with standardized IoT protocols for easy interoperable communication with minimal integration overhead is achieved. At the data layer, we guarantee traceability and auditability and long-term data retention via QR-indexed, metadata-enriched storage structures. The intelligence layer at the end leverages AI-powered analytics for predictive diagnostics, adaptive optimization, and data-driven continuous improvement.

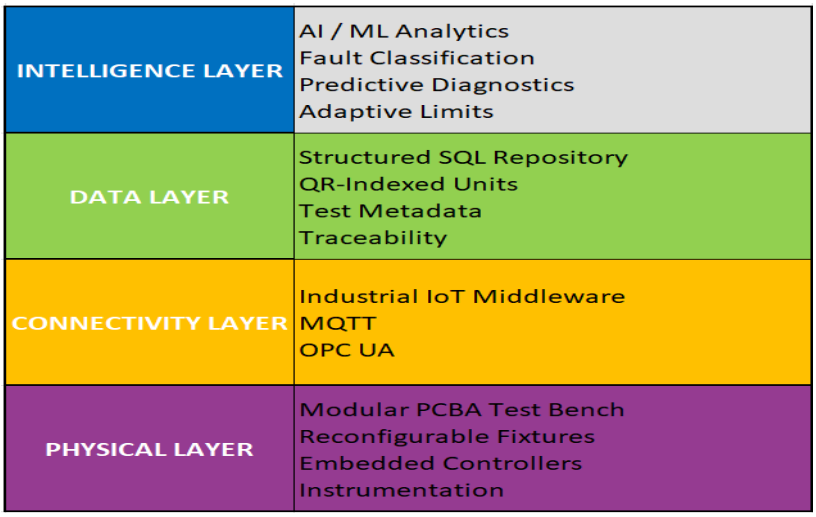

Fig. 1. Conceptual Framework for an IoT-Enabled Cyber-Physical PCBA Test Bench

To strengthen the operational definition of the proposed architecture, the four-layer framework can be represented as a formal cyber-physical systems model rather than only as a conceptual block diagram. The proposed test-bench architecture is defined as: CPTB = {L, I, S, E, D, A}

where L represents the architectural layers, I represents inter-layer interfaces, S represents the operational state set, E represents triggering events, D represents persistent data objects, and A represents admissible control actions. The four architectural layers are defined as follows:

L1: Physical test-execution layer — includes the PCBA unit under test, modular fixture, pogo-pin interface, embedded controller, programmable power supply, sensors, actuators, barcode or QR scanner, and operator-facing test interface. This layer performs deterministic electrical contact, power sequencing, signal acquisition, test execution, and fixture actuation.

L2: Connectivity and communication layer — provides structured communication between the test bench and higher-level information systems using MQTT and/or OPC UA. This layer is responsible for message publication, command routing, acknowledgement handling, timestamping, and communication-status monitoring.

L3: Data-management layer — stores structured production and test data in a SQL database. Each record is indexed using a unique QR-based unit identifier and includes test-script version, firmware version, operator identifier, fixture identifier, timestamp, measured values, pass/fail status, and diagnostic metadata.

L4: Intelligence and optimization layer — applies rule-based analytics and machine-learning models to historical and current test data. This layer generates diagnostic outputs, anomaly indicators, adaptive test recommendations, candidate acceptance-limit adjustments, and engineering actions for fixture or process improvement.

The inter-layer interfaces are defined through explicit communication contracts, as shown in Table 1. These contracts specify the inputs, outputs, direction of information flow, and synchronization behaviour between layers.

The proposed architecture therefore separates deterministic real-time test execution from analytical decision-making. Time-critical operations, such as fixture locking, power sequencing, and measurement acquisition, remain within the physical layer. Analytical outputs from the intelligence layer do not directly override the test bench without a decision gate. Instead, AI-generated outputs are stored as recommendations and are converted into deterministic manufacturing actions only after one of two conditions is satisfied: either the action falls within pre-approved rule limits, such as triggering a retest or flagging a unit for rework, or the action is approved by engineering personnel, such as revising acceptance limits or redesigning fixture interfaces

Table 1: Inter-layer interface contracts of the proposed cyber-physical test-bench architecture

Inter-face	**Direc-tion**	**Input**	**Output**	**Communica-tion semantics**	**Synchronizatio n mechanism**
I1: Physical-to-connect-ivity	L1 -> L2	Raw measurements, fixture status, DUT status, error codes, test-state events	Structured telemetry packet	Event-driven publish/subscri be using MQTT or OPC UA status updates	Timestamp, sequence number, acknowledgeme nt
I2: Connect-ivity-to-physical	L2 -> L1	Test commands, script selection, reset command, retest command, lock/unlock instruction	Local execution response	Command-response or OPC UA method call	Execution acknowledgeme nt and command-state confirmation
I3: Connect-ivity-to-data	L2 -> L3	Validated telemetry, test status, operator metadata, fixture metadata	Stored test record	Asynchronous data ingestion with schema validation	Database transaction commit and write confirmation
I4: Data-to-intelli-gence	L3 -> L4	Historical test records, unit traceability data, measurement trends, fault classifications	Feature set for analytics	Batch or near-real-time data extraction	Query versioning and dataset timestamping

I5: Intelli-gence-to-data	L4 -> L3	Model outputs, anomaly scores, recommended limits, diagnostic labels, confidence values	Stored recommen dation record	Write-back to controlled analytics tables	Model-version and approval-status tracking
I6: Intelli-gence-to-physical via connect-ivity	L4 -> L2 -> L1	Approved test-script change, retest rule, process adjustment, fixture action request	Updated execution instructio n	Closed-loop control only after rule validation or engineering approval	Decision-gate approval, change-log entry, deployment confirmation

To address semantic interoperability, the proposed architecture defines a common information model in addition to communication protocols. While MQTT and OPC UA support data transport, meaningful interoperability requires shared definitions for fixtures, instruments, PCBAs, measurements, calibration states, diagnostic outputs, and analytics recommendations. The semantic model is therefore defined as:
SIM = {NS, OT, MS, EV, H}

where NS represents the namespace structure, OT represents OPC UA object types, MS represents metadata schemas, EV represents controlled enumerations, and H represents the ISA-95 hierarchy.

The OPC UA namespace is organized into four logical groups. The first namespace contains standard OPC UA definitions as shown in Table 2. The second contains ISA-95-aligned equipment, material, personnel, and operations objects. The third contains test-bench-specific entities, including fixtures, embedded controllers, instruments, measurement points, test executions, calibration records, and diagnostic entities. The fourth contains product variants, test scripts, firmware versions, analytics outputs, confidence values, and decision-gate states. This structure allows different subsystems to exchange data using consistent names, units, states, and object relationships.

The model further standardizes measurement, calibration, fault-classification, and analytics-recommendation metadata by defining consistent identifiers, engineering units, result codes, calibration links, diagnostic states, confidence values, and approval states. The main semantic functions of these object types are summarized in Table 2, which provides the common interpretation required for interoperability across the fixture, embedded controller, database, analytics layer, and future MES interface.

The semantic model is also mapped to ISA-95. The manufacturing organization is represented as the Enterprise, the production facility as the Site, the PCBA department as the Area, and the PCBA production line as the ProductionLine. The cyber-physical test bench is mapped to WorkCell/Equipment, while the modular fixture, embedded controller, instruments, sensors, and scanner are mapped to PhysicalAsset or EquipmentModule objects. The PCBA under test is mapped to SerializedMaterial, the

operator to Personnel, the test script to OperationsDefinition/ProcessSegment, the completed test cycle to Operations Performance, and the pass/fail or diagnostic outcome to Quality Test Result.

By defining the semantic layer in this manner, interoperability is no longer limited to protocol compatibility. The architecture establishes a shared meaning for each object, measurement, calibration state, diagnostic condition, and AI recommendation. This allows the physical fixture, embedded controller, SQL database, analytics layer, and future MES interface to interpret data consistently across the complete cyber-physical test-bench architecture.

Table 2: Definition of core OPC UA object types

Object type	Main semantic function
PCBAUnitType	Represents the serialized PCBA under test, including UnitUID, ProductCode, Revision, FirmwareVersion, BatchID, and CurrentStatus.
FixtureType	Represents the modular fixture, including FixtureID, FixtureVersion, PinMapID, ProductCompatibility, FixtureState, and MaintenanceStatus.
EmbeddedControllerType	Represents the local controller responsible for deterministic test execution, heartbeat monitoring, and signal acquisition.
InstrumentType	Represents measurement and control devices, including power supplies, voltage monitors, current sensors, and communication interfaces.
MeasurementPointType	Represents a measured variable, including ParameterCode, EngineeringUnit, NominalValue, LowerLimit, UpperLimit, ActualValue, and ResultCode.
TestExecutionType	Represents a complete test cycle linking the PCBA, fixture, operator, test script, measurement records, and final result.
CalibrationRecordType	Represents calibration validity, including calibration date, due date, offset, gain, uncertainty, and certificate reference.
DiagnosticEntityType	Represents classified faults, including FaultClass, ErrorCode, Severity, RootCauseCandidate, and DiagnosticState.
AnalyticsRecommendationType	Represents AI-generated outputs, including RecommendationType, ModelVersion, ConfidenceValue, ApprovalStatus, and ActionStatus.

The closed-loop execution of the proposed system can be expressed as the following state-transition model:

S = {Idle, Unit_Identified, Fixture_Locked, Test_Configured, Test_Executing, Data_Committed, Result_Classified, Analytics_Queued, Insight_Generated, Decision_Gate, Action_Deployed, Engineering_Review, Fault_Hold}

The operational flow begins in the Idle state. When a QR code is scanned, the system enters Unit_Identified and retrieves the applicable product configuration. Once the unit is physically seated and the fixture is confirmed as closed, the system enters Fixture_Locked. The selected test script, firmware version, product variant, and acceptance limits are then loaded, placing the system in Test_Configured. During Test_Executing, the physical layer performs deterministic measurement and control operations while publishing telemetry and status events to the connectivity layer. After the SQL transaction has successfully written the measurement and metadata records, the system enters Data_Committed. The result is then classified as pass, fail, retest, or diagnostic hold.

Where sufficient data exists, the test record is passed to the intelligence layer through the Analytics_Queued state. The analytics layer evaluates fault patterns, measurement drift, repeated failure modes, and historical limits. This produces the Insight_Generated state, where an analytical output is created. The system then enters a Decision_Gate state. At this point, the output is evaluated according to confidence threshold, action type, risk level, and approval requirement. Low-risk deterministic actions, such as requesting a retest or flagging a unit for rework, may be returned to the physical layer through the connectivity layer. Higher-risk actions, such as modifying test limits, changing test scripts, or redesigning fixture hardware, are routed to Engineering_Review before deployment.

This state model prevents uncontrolled AI intervention in the physical manufacturing process. It ensures that analytical outputs become manufacturing actions only through traceable, version-controlled, and auditable transition paths. The feedback loop is therefore not an informal conceptual relationship but a governed cyber-physical control mechanism with defined states, events, data dependencies, and approval conditions.

The corresponding sequence of information flow is as follows. First, the operator or automated scanner identifies the PCBA through its QR code. Second, the test bench requests the applicable test script, fixture profile, and acceptance limits from the data layer. Third, the physical layer executes the test and publishes structured measurement events through the connectivity layer. Fourth, the data layer commits each measurement record to the SQL database with unit-level traceability metadata. Fifth, the intelligence layer extracts current and historical data to identify trends, repeated faults, abnormal values, or candidate optimization actions. Sixth, the decision gate classifies the recommendation as either an automatic process action, such as retest or rework flagging, or a controlled engineering action, such as limit revision or fixture redesign. Finally, the approved action is written back to the database and, where applicable, deployed to the physical test bench through the connectivity layer.

By defining explicit layers, communication contracts, state transitions, and decision-gated feedback, the proposed architecture becomes more than a conceptual framework. It becomes an implementable cyber-physical execution model whose correctness can be evaluated through state consistency, whose scalability can be evaluated through message throughput and database growth, whose latency can be evaluated at each interface, and whose feasibility can be evaluated through staged implementation using modular fixtures, MQTT or OPC UA communication, SQL storage, and analytics-based optimization.

Most importantly, the framework includes a feedback loop, enabling insights that arrive from analytical models to be fed back into the testing process, the redesign of fixtures, and adjustment of process parameters. Such a feedback mechanism resolves a critical constraint found in previous test-bench architectures in which data were gathered but not systematically used to enhance system performance over time [II], [XI]. The proposed framework closes this loop, matching quality assurance to adaptive manufacturing standards to allow for an organic test bench, capable of adapting itself from production data to the industry as opposed to just being evidence for verification.

The integration of the framework is achieved through a vertically aligned data flow across all layers. The physical layer generates structured measurement data, which is transmitted via the connectivity layer using standardized IoT protocols. The data layer stores and contextualizes this information within indexed repositories. The intelligence layer analyses the stored data and generates actionable insights. These insights are then fed back to the physical layer to refine test execution, fixture design, and process parameters. Together, the layers operate as a unified closed-loop cyber-physical system rather than independent technological components.

In summary, the conceptual framework combines modular hardware design, cost-effective in-house manufacturing, IoT interoperable connectivity, structured data management, and artificial intelligence (AI) analytics under one cyber-physical architecture. This integration directly eliminates the scatteredness that characterizes the present PCBA test-bench approaches, paving the pathways for scalable, SME relevant ground for further empirical validation and industrial adoption.

VII. Conclusions

This study proposes a theoretical approach for a cyber-physical, modular PCBA test bench to meet the development requirements in the field of Industry 4.0 manufacturing. The research provides a systematic basis for designing and modernizing PCBA testing environments through synthesis of common insights from past test-bench architectures, prior use of IoT, cost reduction strategy, and software-centric optimization models. The framework presents the test bench as not simply a separate verification tool, but as an integrated, data-enabled part of the broader manufacturing ecosystem.

The framework serves as a well-rounded concept but remains theoretical and has not yet been empirically validated in production environments. While the proposed architecture is designed to reduce long-term capital and operational expenditure, its deployment within SME contexts may introduce transitional challenges. These include initial integration costs, the need for workforce upskilling in IoT and data analytics,

temporary productivity slowdowns during system migration, and the complexity of retrofitting legacy equipment into standardized communication layers. However, SMEs must balance the trade-off between upfront architectural investment and delayed realization of data-driven optimization benefits. Quantitative demonstrations of cost savings, performance improvements, diagnostic accuracy, and return-on-investment timelines are therefore necessary to substantiate the practical viability of the framework. Future work should also investigate phased deployment strategies that minimize operational disruption while progressively introducing modular hardware, connectivity protocols, structured data repositories, and AI-enabled analytics.

The novelty of the proposed framework lies in its ability to reconcile previously fragmented approaches into a unified test-bench architecture. This architecture is specifically designed to address the technical and economic constraints of small- and medium-scale electronics production. By integrating modular system designs, in-house manufacturing capabilities, Internet of Things-enabled data collection, and AI-driven analytics, the framework creates a route for reduced testing costs, increased process transparency, and increased diagnosis capacity. Such characteristics are significant for SMEs with the intention to introduce principles of Industry 4.0 without facing prohibitive costs for standard, outsourced test infrastructures.

Finally, the research supports the idea that systems adaptability and data intelligence are core to modern PCBA production quality assurance practices. Rigid, stand-alone test benches increasingly fall out of sync with the variability and complexity of modern electronics manufacturing. Such conceptualization of the test bench as a learning-oriented hybrid cyber-physical system would help to close the loop between quality aim and systems design in the manufacturing context, thus establishing a platform for future deployment and continuous improvement. Optimizing a cost-effective in-house manufactured test bench with IoT capability, based on a framework that integrates four specific layers, will prove to be a scientific contribution

VIII. Acknowledgements

The authors wish to gratefully acknowledge the support of Radio Data Communications (Pty) Ltd for providing access to relevant operational information, production-process insights, and technical assistance during the preparation of this paper. The cooperation and practical input received from the company contributed meaningfully to the contextual understanding of the manufacturing and test-bench environment considered in this study. The authors further acknowledge the assistance of the technical and production personnel whose experience and feedback supported the development and refinement of the research presented. Their contributions assisted in ensuring that the study remained grounded in practical industrial requirements and reflected the realities of an operational manufacturing environment.

Conflict of Interest:

The authors declare that there was no relevant conflict of interest regarding this paper.

References

I. Babu, S., et al. "Enhancing Efficiency and Productivity: IoT in Industrial Manufacturing." *Proceedings of the 2023 IEEE 5th International Conference on Cybernetics, Cognition and Machine Learning Applications (ICCCMLA)*, IEEE, 2023, pp. 693-697. 10.1109/ICCCMLA58983.2023.10346807.

II. Balaji, A., et al. "Development of Test Automation Framework for Printed Circuit Board Assembly." *Journal of Physics: Conference Series*, vol. 2070, 2021, article 012142. 10.1088/1742-6596/2070/1/012142.

III. Baumers, M., et al. "Informing Additive Manufacturing Technology Adoption: Total Cost and the Impact of Capacity Utilisation." *International Journal of Production Research*, vol. 55, no. 23, 2017, pp. 6957-6970. 10.1080/00207543.2017.1334978.

IV. Brecher, C., M. Emonts, and M. Weigold. "Modular Production and Testing Systems for Mechatronic Manufacturing." *Procedia Collège International pour la Recherche en Productique*, vol. 96, 2021, pp. 42-48. https://www.sciencedirect.com/journal/procedia-cirp/vol/96/suppl/C.

V. Brecher, C., et al. "Data Usage in the Internet of Production: Development of a Process Database for Data-Driven Modeling." *The International Journal of Advanced Manufacturing Technology*, vol. 141, 2025, pp. 5781-5792. 10.1007/s00170-025-15951-8.

VI. Chen, D., et al. "Smart Factory of Industry 4.0: Key Technologies, Application Case, and Challenges." *IEEE Access*, vol. 6, 2017, pp. 6505-6519. 10.1109/ACCESS.2017.2783682.

VII. Dello Sterpaio, L., et al. "A Complete EGSE Solution for the SpaceWire and SpaceFibre Protocol Based on the PXI Industry Standard." *Sensors*, vol. 19, no. 22, 2019, article 5013. 10.3390/s19225013.

VIII. Fiedler, F., et al. "Jigs and Fixtures in Production: A Systematic Literature Review." *Journal of Manufacturing Systems*, vol. 72, 2024, pp. 373-405. 10.1016/j.jmsy.2023.10.006.

IX. Gouveia, J. R., et al. "Life Cycle Assessment and Cost Analysis of Additive Manufacturing Repair Processes in the Mold Industry." *Sustainability*, vol. 14, no. 4, 2022, article 2105. 10.3390/su14042105.

X. Kibbe, C., J. Lee, and K. Dong. "Designing a Test Fixture with DFSS Methodology." *International Journal of Manufacturing Engineering*, vol. 2016, 2016, article 3848103. 10.1155/2016/3848103.

XI. Kim, D., et al. "Rapid Fault Cause Identification in Surface Mount Technology Processes Based on Factory-Wide Data Analysis." *International Journal of Distributed Sensor Networks*, vol. 15, no. 2, 2019, article 1550147719832802. 10.1177/1550147719832802.

XII. Kokare, S., J. M. Oliveira, and H. A. Almeida. "Life Cycle Assessment of Additive Manufacturing Processes: A Review." *Journal of Manufacturing Systems*, vol. 68, 2023, pp. 536-559. 10.1016/j.jmsy.2023.05.007.

XIII. Ladegourdie, M., and J. Kua. "Performance Analysis of OPC UA for Industrial Interoperability towards Industry 4.0." *IoT*, vol. 3, no. 4, 2022, pp. 507-525. 10.3390/iot3040027.

XIV. Lee, J., B. Bagheri, and H. Kao. "A Cyber-Physical Systems Architecture for Industry 4.0-Based Manufacturing Systems." *Manufacturing Letters*, vol. 3, 2015, pp. 18-23. 10.1016/j.mfglet.2014.12.001.

XV. Li, C., et al. "Research on a Robust Traceability Method for the Assembly Manufacturing Supply Chain Based on Blockchain." *Applied Sciences*, vol. 15, no. 21, 2025, article 11598. 10.3390/app152111598.

XVI. Moayedi, S. "Upgrade of ATLAS Hadronic Tile Calorimeter for the High Luminosity LHC." *Proceedings of Science*, ICHEP2020, 2021, article 860. 10.22323/1.390.0860.

XVII. Narula, S., et al. "Industry 4.0 Implementation in Electronics Manufacturing Industry - A Case Study." *AIP Conference Proceedings*, vol. 2521, no. 1, 2023, article 050007. 10.1063/5.0114770.

XVIII. Naudé, A., and J. H. van Vuuren. "A Machine Learning Framework for Data-Driven Defect Detection in Multistage Manufacturing Systems." *South African Journal of Industrial Engineering*, vol. 35, no. 2, 2024, pp. 154-170. 10.7166/35-2-3008.

XIX. Nkadimeng, E., et al. "A Monitoring and Control Test Bench for Assessing the Upgraded Low Voltage Power Supplies for the ATLAS Tile Calorimeter Phase-II Upgrade Front-End Electronics." *Journal of Instrumentation*, vol. 17, no. 7, 2022, article P07025. 10.1088/1748-0221/17/07/P07025.

XX. Onu, P., A. Pradhan, and C. Mbohwa. "Industrial Internet of Things (IIoT): Opportunities, Challenges, and Requirements in Manufacturing Businesses in Emerging Economies." *Procedia Computer Science*, vol. 217, 2022, pp. 856-865. 10.1016/j.procs.2022.12.282.

XXI. Schuitemaker, R., and X. Xu. "Product Traceability in Manufacturing: A Technical Review." *Procedia CIRP*, vol. 93, 2020, pp. 700-705. 10.1016/j.procir.2020.04.078.

XXII. Shah, M., et al. "Design and Development of Test Bench for Pocket Labs." *Discover Electronics*, vol. 1, 2024, article 25. 10.1007/s44291-024-00030-1.

XXIII. Siddiqui, A., M. Zia, and P. Otero. "A Universal Machine-Learning-Based Automated Testing System for Consumer Electronic Products." *Electronics*, vol. 10, no. 2, 2021, article 136. 10.3390/electronics10020136.

XXIV. Siddiqui, A., P. Otero, and M. Zubair. "A Novel System to Increase Yield of Manufacturing Test of an RF Transceiver through Application of Machine Learning." *Sensors*, vol. 23, no. 2, 2023, article 705. 10.3390/s23020705.

XXV. Sitcharangsie, S. "Evaluating Industry 4.0 Readiness and Investment Feasibility in an SME Industrial Factory." *2024 IEEE International Conference on Industrial Engineering and Engineering Management (IEEM)*, IEEE, 2024, pp. 1199-1203. 10.1109/IEEM62345.2024.10857062.

XXVI. Stoyanov, S., et al. "Predictive Analytics Methodology for Smart Qualification Testing of Electronic Components." *Journal of Intelligent Manufacturing*, vol. 30, 2019, pp. 1497-1514. 10.1007/s10845-018-01462-9.

XXVII. Verani, A., et al. "Modular Battery Emulator for Development and Functional Testing of Battery Management Systems: Hardware Design and Characterization." *Electronics*, vol. 12, no. 5, 2023, article 1232. 10.3390/electronics12051232.

XXVIII. Wang, L., Y. He, and Z. Wu. "Design of a Blockchain-Enabled Traceability System Framework for Food Supply Chains." *Foods*, vol. 11, no. 5, 2022, article 744. 10.3390/foods11050744.

XXIX. Yang, F., and S. Gu. "Industry 4.0, a Revolution That Requires Technology and National Strategies." *Complex & Intelligent Systems*, vol. 7, 2021, pp. 1311-1325. 10.1007/s40747-020-00267-9.

XXX. Yang, Z., Q. Wang, and M. Jia. "Integrating Industry 4.0 and the Internet of Things (IoT) for Eco-Friendly Manufacturing." *The International Journal of Advanced Manufacturing Technology*, vol. 129, no. 9-12, 2023, pp. 4567-4583. 10.1007/s00170-023-12331-y.

XXXI. Zheng, C., et al. "SME-Oriented Flexible Design Approach for Robotic Manufacturing Systems." *Journal of Manufacturing Systems*, vol. 53, 2019, pp. 62-74. 10.1016/j.jmsy.2019.09.010