JOURNAL OF MECHANICS OF CONTINUA AND MATHEMATICAL SCIENCES
www.journalimcms.org

ISSN (Online) : 2454 -7190 Vol.-21, No.-05, May (2026) pp 109-124 ISSN (Print) 0973-8975

A HIGH STEP-UP COUPLED INDUCTOR DC-DC CONVERTER FOR GRID CONNECTED SOLAR PHOTOVOLTAIC SYSTEMS

Biswamoy Pal[1], Milan Sasmal[2], Partha Das[3], Anik Kar[4], Shib Sankar Saha[5], Sudip Das[6]

[1, 2, 3, 4] Electrical Engineering Department, JIS College of Engineering, India-741235.

[5] Electrical Engineering Department, Kalyani Government Engineering College, India-741235.

[6] Electrical Engineering Department, Swami Vivekananda University, India-700121.

Email: [1]biswamoy.paul@jiscollege.ac.in, [2]milan.sasmol@jiscollege.ac.in, [3]partha.das@jiscollege.ac.in, [4] anik.kar32@gmail.com, [5]sahashib@hotmail.com, [6]sudipdas1380@gmail.com

Corresponding Author: **Biswamoy Pal**

https://doi.org/10.26782/jmcms.2026.05.00008

(Received: February 24, 2026; Revised: May 04, 2026; Accepted : May 12, 2026)

Abstract

This paper presents a coupled inductor-based high-gain DC-DC converter. The proposed topology achieves high step-up conversion and reduced voltage stress of the switch and output diode. The leakage energy is recycled effectively to improve converter efficiency. Moreover, huge turn-off voltage spikes of the switch caused by the leakage inductor are completely eliminated. Besides, all the diodes, except the output diode, turn off softly, eliminating the reverse recovery problem. The operating principle of the converter in continuous conduction mode (CCM) is presented. The voltage gain characteristics, CCM-DCM boundary operation, and parameter design guidelines have been elaborated. A comparison analysis with similar converters has also been presented. Finally, the theoretical analysis has been verified through a simulation study in orcad pspice software. The simulation results are found to be in close agreement with the theoretical calculations.

Keywords: Boost converter, continuous conduction mode (CCM), coupled Inductor, discontinuous conduction mode (DCM), solar photovoltaic (SPV), zero current switching (ZCS).

I. Introduction

The deployment of grid-connected SPV systems has been accelerated over the years to reduce carbon emissions and the depletion of natural resources.

Although photovoltaic (PV) is a promising renewable energy resource that provides clean electricity generation, unfortunately, this source produces electricity with very low and fluctuating output voltage [XXV]. Thus, a grid-connected SPV system essentially needs a high gain DC-DC converter to match the required voltage level [III], [XI], [XXI], [XX]. Fig. 1 depicts the architecture of a grid-connected SPV system. Conventional DC-DC converters with voltage boosting capabilities, such as boost, buck-boost, cuk, and sepic, offer limited voltage gain and need to operate at extreme duty ratios to improve voltage gain [XIX]. Converters operating with a large duty ratio lead to poor efficiency and high device stress [VI].

Transformer-based isolated DC-DC converter topologies are very attractive to offer high voltage gain without extreme duty ratio operation. These converters achieve high gain by increasing the transformer's turns ratio and provide inherent input-output galvanic isolation. Among isolated converters, flyback and forward converter topologies are popular due to their simple structures and low component counts [XIX]. However, these converters are restricted to low-power applications. Half-bridge and full-bridge DC-DC converters [II] are capable of handling high power, but use a large number of semiconductors, making it costlier and increasing the gate driver requirement. Moreover, the transformer-based converters suffer from a serious issue, such as high voltage stress across the switch at turn-off due to the presence of leakage inductance[IX], [XII], [IV], [VII]. This necessitates the use of a high-voltage semiconductor switch with high switch-on state resistance ($R_{DS,\,on}$), leading to significant conduction loss. Moreover, the converter reliability is compromised. To address this issue,[XXIV], [XIII], and [XIV] have added active clamping networks with the conventional converters at the cost of increased component count and structural complexity. The leakage inductance is further aggravated by increasing the transformer's turn ratio. Thus, a higher turns ratio provides high output voltage, while compromising device stress and leakage inductance.

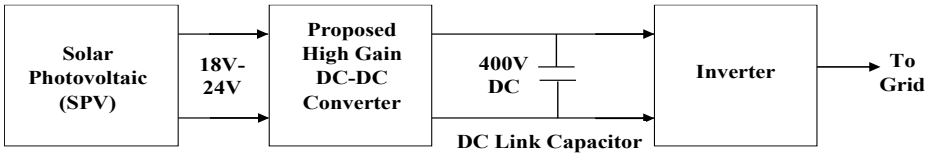


Fig. 1. Schematic of a grid-connected SPV system

To avoid leakage inductance effect, many non-isolated high-gain topologies that use no transformer have been presented [XVII], [XXII], [XXVI], [V], [XVI], [X], [XVIII]. All these converters can achieve a high step-up voltage conversion ratio, but excessive device stress and higher conduction loss in the second stage of [XVII], reverse recovery issue in diodes in [XXII], [XXVI], [V], [XVI], [X], [XVIII] are the major limitations. Besides, the use of two switches in converters [XVII], [XXII], [XXVI], [V], [XVI], [X] increases cost and control complexity. Moreover, a large number of passive elements have been employed in all these converters to ensure high voltage gain. In [VIII], [XV], [I], a combination of coupled inductors and fewer energy-storing elements has been used to achieve high voltage gain. The leakage

energy issues in [VIII], [XV] have been handled efficiently, whereas [I] does not provide any leakage recovery mechanism. However, the use of extra switches in [VIII], [I] increases topological and gate driver complexity.

In this work, a single-switch high-gain coupled inductor DC-DC converter is proposed. The converter achieves high voltage gain without operating the converter at an extreme duty ratio. The notable features of the proposed topology include: 1) low component count, 2) high voltage gain, 3) reduced voltage stress on switch and output diode, 4) efficient leakage energy recovery, 5) reduced reverse recovery loss of diodes, 6) reduced-sized output capacitor, 7) high efficiency.

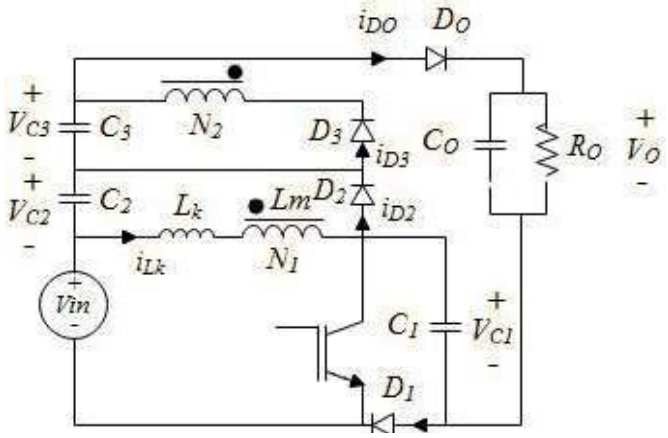


Fig. 2. Circuit diagram of the proposed converter

II. Circuit Description and Converter Operation

The circuit diagram of the proposed high-gain DC-DC converter is presented in Fig. 2. The proposed converter replaces the boost inductor of the conventional boost converter by a coupled inductor having primary and secondary turns of N_1 and N_2, respectively. The primary inductance of the coupled inductor is L_m, and L_k is the leakage inductance referred to the primary side. The main objective of employing a coupled inductor is to achieve high voltage gain. Apart from the coupled inductor, the proposed converter comprises a switch (S_W), output diode (D_O), and output capacitor (C_O) to form a boost converter configuration. Additionally, three capacitors ($C_1 - C_3$) and three diodes ($D_1 - D_3$) are used to further elevate the voltage gain.

The converter operation is described below with the following assumptions.

- All semiconductor devices have zero on-state resistance.
- The magnetizing inductance (L_m) is large enough to maintain constant current, and the coupled inductor operates in continuous conduction mode (CCM).
- The capacitors (C_O–C_3) are large enough to maintain ripple-free voltages.
- The leakage inductance (L_k) is much smaller than L_m, and k represents the coefficient of coupling.

Before the turn-on of S_W, D_O, D_1, *and* D_2 are in the off state. The stored magnetizing energy of the coupled inductor is transferred to C_3 through the diode D_3. The load is delivered by the stored energy of the output capacitor (C_O). The converter operation is completed in 4 operating modes. The equivalent circuit in each operating mode is depicted in Fig.3, and the key waveforms are shown in Fig.4. The notations T_{SW} and f_{SW} represent switching time period and switching frequency, respectively. The operating modes of the proposed converter are explained below.

Mode 1(t_0– t_1): This mode begins with the turn-on of the switch (S_W) and the diode D_O gets forward-biased. Now, the load is supplied by the series combination of V_{in}, V_{C2}, $V_{C3,}$ and V_{C1} through the switch and output diode. As the diode D_3 is already conducting, a constant voltage of V_{C3}/n is impressed across L_m, while L_k experiences a voltage of $V_{in}+V_{C3}/n$. Thus, the leakage inductor current (i_{Lk}) increases linearly, and consequently, the current i_{D3} decreases in the same fashion. This mode ends when i_{Lk} reaches the value I_{Lm} and D_3 turns off under zero current switching (ZCS). The circuit variables and mode duration may be expressed as,

$$i_{Lk}(t) = \frac{V_{in} + V_{C3}/n}{L_k}(t - t_0) \tag{1}$$

$$\Delta t_{01} = t_1 - t_0 = \frac{I_{Lm} L_k}{V_{in} + V_{C3}/n} \tag{2}$$

Where, n= N_2 / N_1

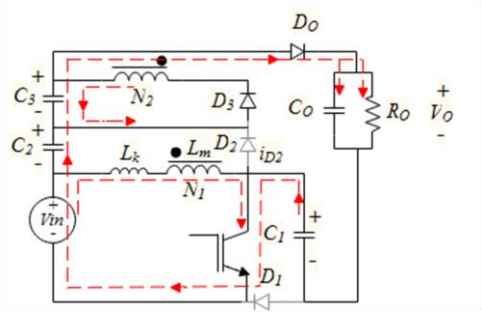
$$V_O = V_{in} + V_{C1} + V_{C2} + V_{C3} \tag{3}$$

Mode 2 (t_1 – t_2): During this mode, the load is supplied by the input and the capacitors as before. The leakage and magnetizing inductors are energized by the input. This mode ends with the turn off of the switch.

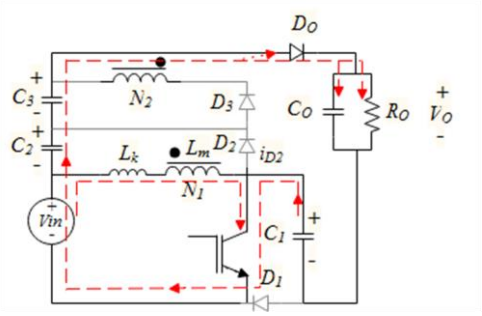
$$i_{Lk}(t) = I_{Lm} \tag{4}$$

$$\Delta t_{12} = t_2 - t_1 = D / f_{SW} - \Delta t_{01} \tag{5}$$

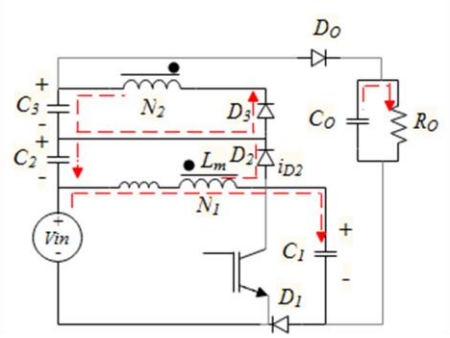
Mode 3 (t_2 – t_3): As the gate pulse of S_W is withdrawn at t_2, the stored leakage and magnetizing energy are transferred to C_1, C_2, and C_3 through D_1, D_2, and D_3, respectively. During this mode, the current i_{Lk} decreases, while i_{D3} increases. This mode ends when i_{Lk} is decreased to zero and the diodes D_1 and D_2 commutate under ZCS conditions. The load is supplied by the output capacitor in this mode.



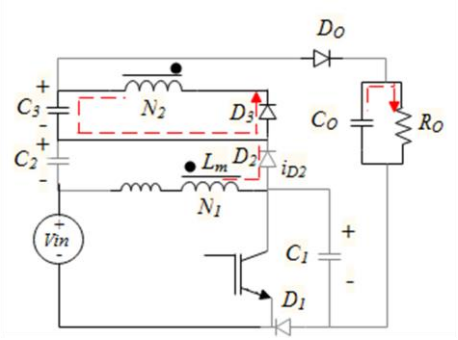
(a) Mode 1 (t_0-t_1)



(b) Mode 2 (t_1-t_2)



(c) Mode 3 (t_2-t_3)



(d) Mode 4 (t_3-t_4)

Fig. 3. Equivalent circuits in each operating mode

$$i_{Lk}(t) = I_{Lm} - \frac{V_{C2} - V_{C3}/n}{L_k}(t - t_2) \tag{6}$$

$$\Delta t_{23} = t_3 - t_2 = \frac{I_{Lm} L_k}{V_{C2} - V_{C3}/n} \tag{7}$$

$$V_{C1} = V_{in} + V_{C2} \tag{8}$$

$$V_{C3} = knV_{C2} \tag{9}$$

Mode 4($t_3 - t_4$): This is the passive mode of the converter operation. During this mode, the stored magnetizing energy is delivered to C_3, while the load is supplied by C_O. This mode ends with the turn-on of S_W again, and the next switching cycle gets started.

$$\Delta t_{34} = t_4 - t_3 = (1 - D)/f_{SW} - \Delta t_{23} \tag{10}$$

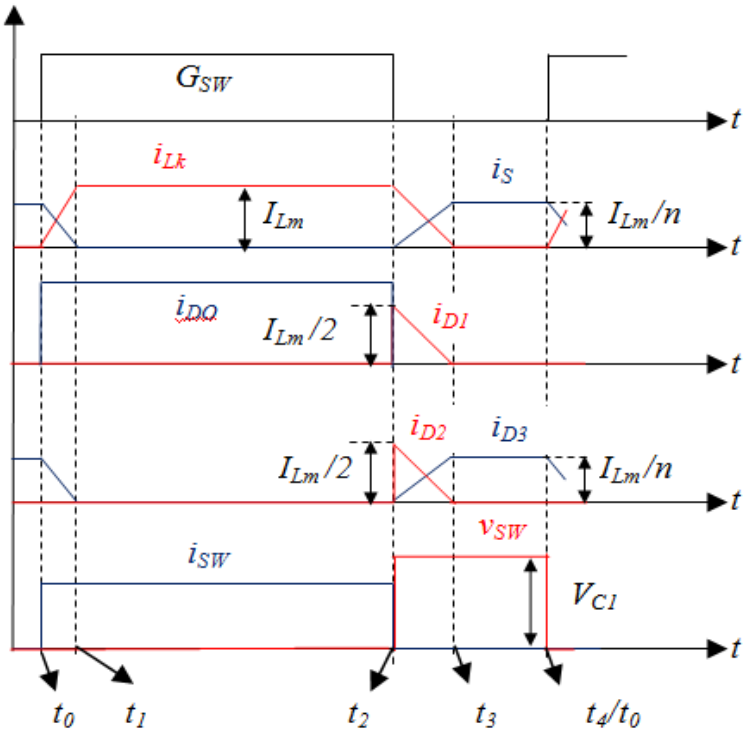


Fig. 4. Key waveforms

III. Steady State Analysis

This section describes a detailed analysis of voltage gain, CCM-DCM boundary condition, and device stress.

A. Voltage Gain

As described in the operating principle of the converter, during the mode duration (Δt_{01}), the switch current increases slowly due to the presence of leakage inductance, and that through D_3 (i_S=i_{D3}) decreases. As D_3 conducts during this period, the secondary winding of the coupled inductor gets V_{C3} voltage across it. It is worth mentioning that the capacitor C_3 is large enough to maintain a constant voltage of V_{C3}. Thus, the primary winding (L_m) of the coupled inductor gets a constant reflected voltage V_{C3}/n during Δt_{01}. However, at t_1 ad D_3 stops conducting, and S_W is already in conduction, a voltage kV_{in} is impressed across L_m until the switch is turned off. Again, at t_2, when the switch is turned off, the diode D_3 starts conducting again; consequently, current through it increases gradually due to the presence of L_k and reaches its peak value at t_3. Due to CCM operation, the diode D_3 conducts for the entire turn-off duration ($t_2 - t_4$) of the switch, and thus, the voltage impressed across L_m is V_{C3}/n. The expression of voltage across L_m is expressed mathematically for different mode intervals in (11).

$$\begin{cases} v_{Lm} = kV_{in}; & t_1 \le t \le DT_{SW} \\ = V_{C3}/n; & 0 < t \le t_1 \text{ and } DT_{SW} \le t \le T_{SW} \end{cases} \tag{11}$$

Applying the volt-second balance principle to L_m and using (11), the expression of V_{C3} may be obtained as,

$$V_{C3} = nkV_{in}\frac{D-\Delta t_{01}f_{SW}}{(1-D)+\Delta t_{01}f_{SW}} \tag{12}$$

Combining (3), (8), (9), and (12), the expression of the voltage gain of the proposed converter is expressed as

$$G_V = \frac{V_O}{V_{in}} = 2+(2+nk)\frac{D-\Delta t_{01}f_{SW}}{(1-D)+\Delta t_{01}f_{SW}} \tag{13}$$

From (13), it is clear that the voltage gain of the converter depends on n, D, k, and Δt_{01}. The terms k and Δt_{01} introduced in the gain equation represent the effect of L_k on converter gain. It is worth mentioning that the leakage inductance (L_k) may be neglected if the following conditions are true.

i. Use of interleaved winding of the coupled inductor for tight coupling (k≈1).

ii. Leakage dynamics are settled within a very small fraction of the switching time period. Mathematically, $\Delta t_{01} << T_{SW}$.

iii. Leakage energy per cycle is negligible compared to output power.

Under the above circumstances, the voltage gain equation of (13) may be simplified considering k=1 and Δt_{01}=0, as below,

$$G_V = \frac{V_O}{V_{in}} = 2+(2+n)\frac{D}{(1-D)} \tag{14}$$

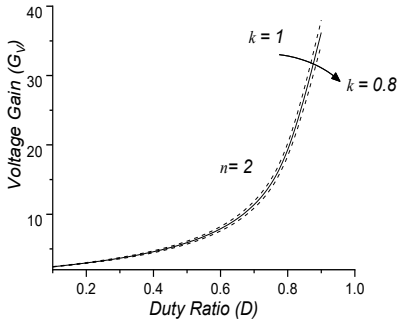


Fig. 5. Voltage gain Vs duty ratio

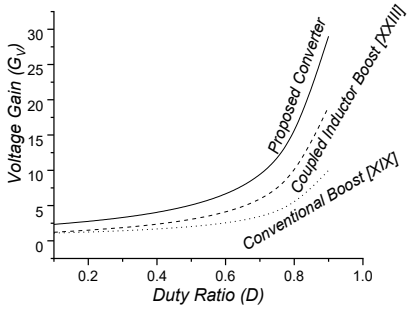


Fig. 6. Voltage gain comparison

Fig. 5 depicts the voltage gain variation with duty ratio for different coupling coefficients. It is clearly observed from the figure that the loose coupling leads to reduced voltage gain; however, the effect of the coupling coefficient on voltage gain is

not very significant. Fig. 6 shows the superiority of the proposed converter in terms of voltage gain compared to the conventional boost converter and the coupled inductor boost converter.

B. CCM-DCM Boundary

Assuming no losses during power conversion, the average input current may be given by,

$$I_{in} = G_V I_O \tag{15}$$

Again, the expression of average input current may also be expressed as,

$$I_{in} = \left(I_{Lm} + I_O\right)D + I_{Lm}\left(1-D\right)/2 \tag{16}$$

From (15) and (16), the expression of magnetizing current may be expressed as,

$$I_{Lm} = \frac{2\left(G_V - D\right)I_O}{D+1} \tag{17}$$

The ripple magnetizing current may be approximated as,

$$\Delta I_{Lm} = \frac{V_{in}D}{L_m f_{SW}} \tag{18}$$

CCM operation of the converter is ensured if the following condition is satisfied.

$$\Delta I_{Lm} < 2I_{Lm} \tag{19}$$

From (17) – (19), the expression of the normalized time constant (τ_C) is obtained as follows.

$$\tau_C = \frac{L_{m1}}{R_O} f_{SW} = \frac{D(1+D)}{2G_V(G_V - D)} \tag{20}$$

The effect of turn ratio on normalized time constant is shown in Fig. 7. An increase in turn ratio (n) reduces the normalized time constant. This implies, at a higher value of n, in fact, less inductance is required to maintain CCM operation of the

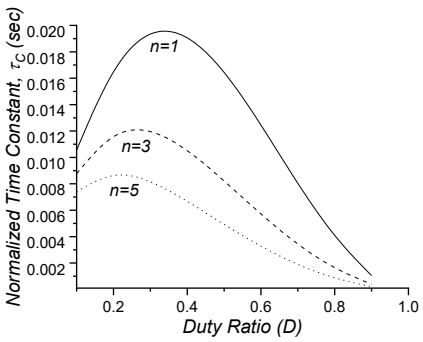


Fig. 7. τ_C Vs D for different n

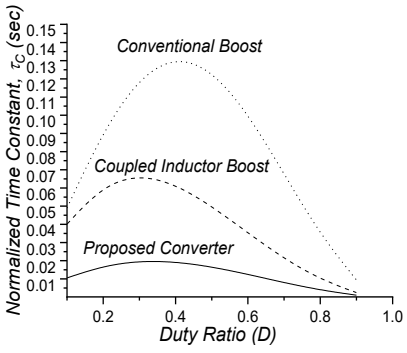


Fig. 8. Comparison of τ_C

converter. The requirement of less inductance in the proposed converter compared to conventional and coupled inductor boost is evident from Fig. 8.

C. Device Stress

The voltage stress on the semiconductor devices of the proposed converter is depicted in Table I under ideal conditions. However, other than leakage inductance, a practical converter includes several parasitics, such as switch parasitic capacitance, ESR, ESL, and diode reverse recovery. These parasitic elements cause transient overvoltage to occur during the switching transition.

Nevertheless, the use of an efficient clamp circuit and soft turn-off of all the diodes minimizes this transient overvoltage. Although ESL in the path (C_1-D_1) would cause a transient overvoltage on the switch, this ESL can be greatly reduced by reducing the PCB track length between the switch collector terminal and diode anode terminal in real-time hardware.

Thus, with a careful PCB layout design, the proposed converter topology experiences negligible transient voltage overshoot. However, as a common practice, a margin of safety of the voltage rating must be considered while selecting semiconductors.

IV. Design Guidelines

This section provides brief design guidelines for selecting circuit components. The circuit parameters have been selected based on the converter specifications as detailed in Table II.

Table 1: Voltage Stress on Semiconductor Devices

Power Device	Voltage Stress
Switch (S_W)	$\frac{V_{in}}{1-D}$
Diode (D_O, D_1, D_2)	$\frac{V_{in}}{1-D}$
Diode (D_3)	$\left(\frac{1}{1-D}+n\right)V_{in}$

Table 2: Converter specifications

Parameters	Specifications
Input Voltage (V_{in})	22V – 26V
Output Voltage (V_O)	400V
Output Power (P_O)	400W
Switching Frequency (f_{SW})	40kHz

A. Selection of Coupled Inductor Parameters (L_m and n)

It is worth mentioning that a higher turns ratio (n) of the coupled inductor of the proposed converter, although it increases voltage gain without operating at extreme duty ratio, leads to increased leakage inductance, large voltage stress across D_3, and higher conduction loss. A suitable value of $n = 2$ is selected in this paper to achieve the desired voltage gain and simultaneously restrict the voltage stress of D_3 well below half of the output voltage.

Using Fig. 7, the critical value of magnetizing inductance is found to be 170μH to operate the converter in CCM upto 20% of the rated load. It is well observed from Fig.9 that at this inductance value, the % ripple magnetizing current is below 15%. Thus, a suitable value of L_m = 175μH is selected in this paper to facilitate wide load range CCM operation and simultaneously, retaining % ripple current below 15%.

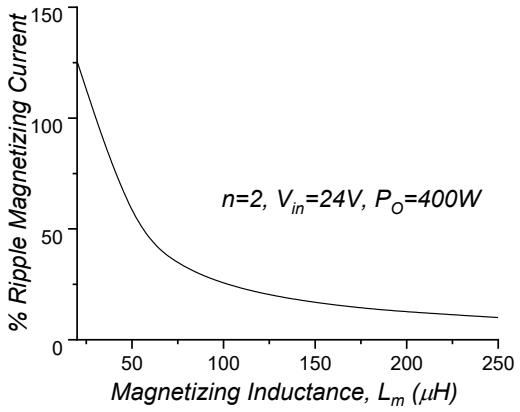


Fig. 9. Ripple magnetizing current variation with L_m

B. Selection of Capacitors (C_1, C_2, C_3, C_O)

The expression of ripple voltages across the capacitors (C_1, C_2, C_3) are given by,

$$\begin{cases} \Delta v_{C1} = \dfrac{I_{Lm}(1-D)}{4C_1 f_{SW}} \\ \Delta v_{C2} = \dfrac{I_{Lm}(1-D)}{4C_2 f_{SW}} \\ \Delta v_{C3} = \dfrac{I_{Lm}(1-D)}{nC_3 f_{SW}} \end{cases} \tag{21}$$

Using the above expressions, the capacitor (C_1, C_2, C_3) values are calculated to be 27μF, 33.9 μF, and 38.6μF, respectively, such that the voltage ripple of respective capacitors is restricted to 1% of their respective voltages. Thus, C_1 and C_2 are selected as 33μF, whereas C_3 = 57μF is chosen in this paper.

The expression of ripple voltage across the capacitor (C_O) is given by,

$$\Delta v_{CO} = \frac{I_O(1-D)}{C_O f_{SW}} \tag{22}$$

From (22), the output capacitor is chosen to be 33 µF.

V. Comparison

A detailed comparative analysis of the proposed converter is given in Table III. It is observed that the proposed converter uses fewer components than other converters, except [I]. However, [I] employs three semiconductor switches, which increases converter cost, gate driver requirement, and control complexity. Although [XVI] has the same total component count as the proposed converter, but uses a more controlled switch. A voltage gain comparison of the converters presented in Fig. 10 clearly shows that the converters [XXVI], [XVI], and [XVIII] offer better voltage gain profiles at low duty ratios; however, their operation is applicable up to a limited duty ratio. As clearly observed from Fig. 10, among the converters with wide duty ratio operation, only [X] has a better voltage gain profile than the proposed converter, but at the cost of a huge number of component employment. The main switch voltage stress comparison, as depicted in Fig. 11, shows that the proposed converter's main switch experiences reduced voltage stress than others; however, at extreme duty ratio, [XXII], [X] offer less stress. The superiority of the proposed converter in terms of output voltage stress is evident from Fig. 12. All these distinguished features enable the converter to operate with a high efficiency of 95.4% at full load conditions.

Table 3: Comparison of similar converters

Ref	No. of Elements	Total Component count	Voltage Gain (Gv)	Switch Voltage Stress	Output Diode Voltage Stress	Efficiency
[XXII]	2S, 4D, 2L, 4C	12	$\frac{4}{1-D}$	$\frac{V_O}{4}, \frac{V_O}{2}$	$\frac{V_O}{2}$	96.5% at 200W
[XXVI]	2S, 4D, 2L, 4C	12	$\frac{2(1-D)}{1-3D+D^2}$	$\frac{D}{1-3D+D^2}V_{in}, \frac{1-D}{1-3D+D^2}V_{in}$	$\frac{1-D}{1-3D+D^2}V_{in}$	92.6% at 120W
[XVI]	2S, 4D, 1L, 3C	10	$\frac{3-2D}{1-2D}$	$\frac{V_{in}}{1-D}$	$\frac{2V_{in}}{1-D}$	95.4% at 198W
[X]	2S, 7D, 4L, 5C	18	$\frac{7+D}{1-D}$	$\frac{1+D}{3+5D}V_O, \frac{1+D}{3+5D}V_O$	$\frac{4}{7+D}V_O$	95.2% at 120W
[XVIII]	1S,5D,3L ,7C	16	$\frac{2+D}{1-2D}$	$\frac{V_{in}}{1-2D}$	$\frac{V_{in}}{1-2D}$	91.3% at 150W
[VIII]	2S, 2D, 1L,1CL, 6C	12	$\frac{1+n}{1-D}$	$\frac{V_{in}}{1-D}, \frac{V_{in}}{1-D}$	$V_o - \frac{V_{in}}{1-D}$	96.4% at 200W

[I]	3S, 1CL, 3C	7	$\frac{2+n-D}{1-D}$	$\frac{V_{in}}{1-D}, V_O - V_{in}, V_O - V_{in}$	$\frac{V_{in}(1+n)}{1-D}$	96% at 3200W
[P]	1S,4D,1CL,4C	10	$2+(2+n)\frac{D}{(1-D)}$	$\frac{V_{in}}{1-D}$	$\frac{V_{in}}{1-D}$	95.4% at 400W
S: Switch, D: Diode, L: Inductor, CL: Coupled Inductor, C: Capacitor						

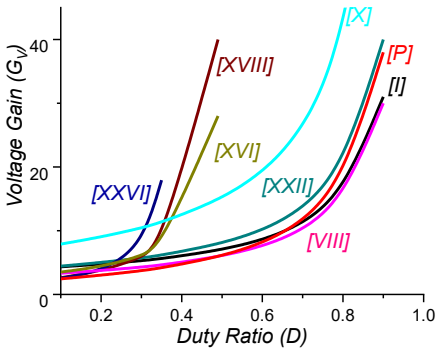


Fig. 10. Voltage gain comparison

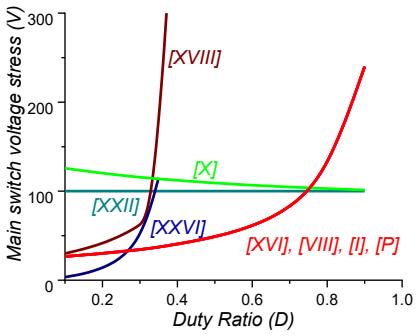


Fig. 11. Main switch voltage stress comparison

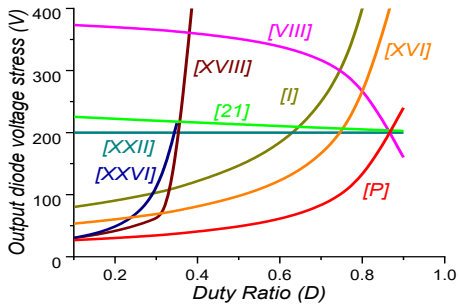


Fig. 12. Output diode voltage stress comparison

Table 4: Converter parameters

Parameters	Specifications
Coupled Inductor (L_m)	175µH
Turns Ratio (n)	2
Capacitors (C_O, C_1, C_2)	33 µF
Capacitors (C_3)	57 µF

VI. Results and Discussions

The converter performance has been validated through a simulation study in orcad pspice with the specifications detailed in Table II and Table IV. Fig. 13 (a) shows the gate pulse waveform and input-output voltage waveform to support the claim of high voltage gain within the permissible duty ratio. The switch voltage and current waveforms are shown in Fig. 13(b). The waveform of switch voltage clearly shows that its voltage stress is equal to V_{C1} as mentioned in Table I. The claims of ZCS turn off all the diodes, except the output diode (D_O), which is evident from Fig. 13(c). Finally, the simulation results of capacitor voltages have been shown in Fig. 13(d). It shows the contribution of each capacitor to the voltage gain of the converter.

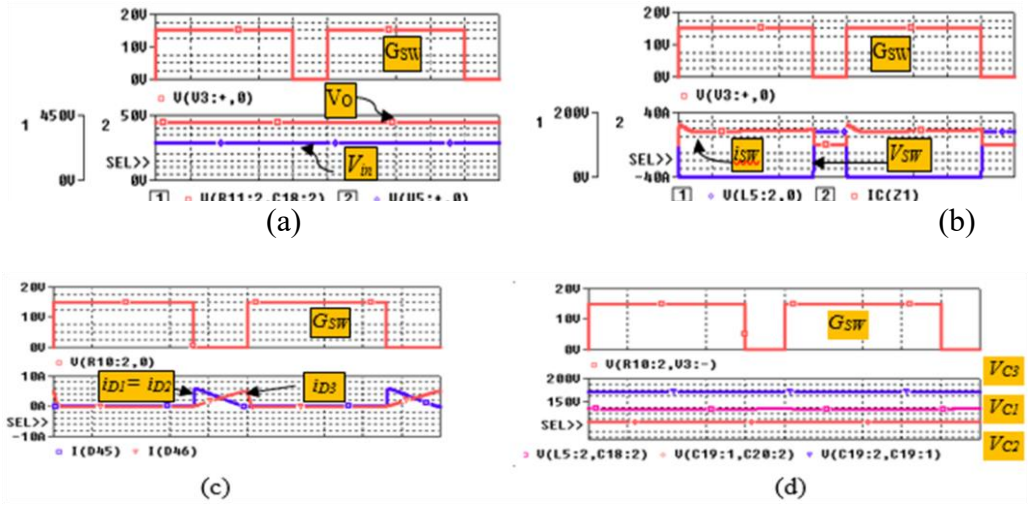


Fig. 13. Simulation results for V_{in} =*24V* at full load; (a) Gate Pulse (G_{SW}), Input voltage (V_{in}), Output voltage (V_O) ; (b) Gate Pulse (G_{SW}), Switch voltage (V_{SW}), Switch current (i_{SW}); (c) Gate Pulse (G_{SW}), Diode currents (i_{D1}, i_{D2}, i_{D3}) (d) Gate Pulse (G_{SW}), Capacitor voltages (V_{C1}, V_{C2}, V_{C3})

VII. Conclusion

A single-switch high-gain DC-DC converter is presented in this work. The converter achieves high voltage gain using minimal components, without operating the converter at an extreme duty ratio. The voltage stress on the semiconductor devices has been significantly reduced. The soft recovery of the diodes ensures high efficiency operation. Detailed operating principle, steady state analysis, and design example have been verified using a simulation study on a 24V/400V, 400W converter. The simulation results are in close agreement with the theoretical calculations. A peak efficiency of the converter is found to be 95.4% at full load conditions.

Conflict of Interest:

The authors declare no conflicts of interest regarding this paper.

References

I. Ayachit, S. U. Hasan, Y. P. Siwakoti, M. Abdul-Hak, M. K. Kazimierczuk and F. Blaabjerg (2019). Coupled-Inductor Bidirectional DC-DC Converter for EV Charging Applications with Wide Voltage Conversion Ratio and Low Parts Count, *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, pp. 1174-1179. 10.1109/ECCE.2019.8912858.

II. C. -L. Chu and Y. Chen (2009). ZVS-ZCS bidirectional full-bridge DC-DC converter, *2009 International Conference on Power Electronics and Drive Systems (PEDS)*, Taipei, Taiwan, pp. 1125-1130. 10.1109/PEDS.2009.5385685.

III. D. Kumar, F. Zare, and A. Ghosh (2017). DC microgrid technology: Systemarchitectures, AC grid interfaces, grounding schemes, power quality, communication nnetworks, applications, and standardizations aspects, *IEEE Access*, vol. 5, pp. 1223012256.

IV. Finney S.J,Williams B.W, Green T.C (1996). RCD snubber revisited. 768 IEEE Trans Ind Appl 32(1):155–160. 10.1109/28.485827.

V. F. Abbasi, Aghdam Meinagh, J. Yuan, and Y. Yang (2020). Analysis and design of a high voltage-gain quasi-Z-source DC–DC converter, *IET Power Electronics*, early access. 10.1049/iet-pel.2019.1165.

VI. Heris PC, Saadatizadeh Z, Rostami N (2019). Transformerless quadratic-based high step-down DC–DC converter with wide duty cycle range, *IET Power Electron.* 12(3):368-382.

VII. H. K. Patel (2008). Voltage transient spikes suppression in flyback converter using dissipative voltage snubbers, *3rd IEEE conference on industrial electronics and applications, Singapore*, 897–901. 10.1109/ICIEA.2008.4582645.

VIII. H. -L. Do (2010). A Soft-Switching DC/DC Converter With High Voltage Gain, *IEEE Transactions on Power Electronics*, vol. 25, no. 5, pp. 1193-1200. 10.1109/TPEL.2009.2039879.

IX. H. Terashi and T. Ninomiya (2004). Analysis of leakage-inductance effect in a flyback DC-DC converter using time keeping control, *INTELEC 2004. 26th Annual International Telecommunications Energy Conference*, Chicago, IL, USA, pp. 718-724. 10.1109/INTLEC.2004.1401550.

X. J. Gnanavadivel, K. Jayanthi, S. Vasundhara, K.V. Swetha& K. JeyaKeerthana (2023). Analysis and design of high gain DC-DC converter for renewable energy applications, *Automatika*, 64:3, 408-421. 10.1080/00051144.2023.2170062.

XI. K. Kobayashi, H. Matsuo, and Y. Sekine (2006). Novel solar-cell power supplysystem using a multiple-input DC–DC converter, *IEEE Trans. Ind.Electron*., vol. 53, no. 1, pp. 281–286.

XII. K. P. Bhatt, M. T. Shah, V. Patel and V. Kharbikar (2011). Effect of leakage inductance in bidirectional DC to DC converter, *2011 Nirma University International Conference on Engineering*, Ahmedabad, India, pp. 1-6. 10.1109/NUiConE.2011.6153303.

XIII. Liang T-J, Huynh KKN, Chen K-H, HuangW-Y, Tran TAA (2024). Forward–flyback integrated converter with voltage clamping and soft switching, *IEEE Trans Power Electron* 39(10):13365–13376. 10.1109/TPEL.2024.3418491

XIV. Lin JY, Wang CF, Lin CY, Chen JL, Wang JM (2014). An active clamping zero-voltage-switching flyback converter with integrated transformer, *Int J Circuit Theory Appl* 43(10):1351–1366. 10.1002/cta.2009.

XV. Lish, M. H., Ebrahimi, R., Kojabadi, H. M., Guerrero, J. M., Esfetanaj, N. N., & Chang, L. (2020). Novel high gain DC–DC converter based on coupled inductor and diode capacitor techniques with leakage inductance effects. IET Power Electronics, 13(11), 2380-2389. 10.1049/iet-pel.2020.0117.

XVI. M. -K. Nguyen, T. -D. Duong and Y. -C. Lim (2018). Switched-Capacitor-Based Dual-Switch High-Boost DC–DC Converter, *IEEE Transactions on Power Electronics*, vol. 33, no. 5, pp. 4181-4189. 10.1109/TPEL.2017.2719040.

XVII. M. Lotfi Nejad, B. Poorali, E. Adib, and A. A. Motie Birjandi (2016). New cascade boost converter with reduced losses, *IET Power Electronics*, vol. 9, no. 6, pp. 1213–1219. 10.1049/iet-pel.2015.0240.

XVIII. M. M. Haji-Esmaeili, E. Babaei and M. Sabahi (2018). High Step-Up Quasi-Z Source DC–DC Converter, *IEEE Transactions on Power Electronics*, vol. 33, no. 12, pp. 10563-10571. 10.1109/TPEL.2018.2810884.

XIX. N. Mohan, T.M. Undeland and W.P. Robbins (2003). Power Electronics: Converters, Applications and Design, *3rd edition, Hoboken, NJ, USA, Wiley*:*2003*, ISBN 978-0-471-22693-2.

XX. P. K. Maroti, S. Esmaeili, A. Iqbal, and M. Meraj (2020). High step-up single switch quadratic modified SEPIC converter for DC microgrid applications, *IET Power Electron*., vol. 13, no. 16, pp. 37173726. 10.1049/iet-pel.2020.0147.

XXI. S. K. Mazumder, R. K. Burra, and K. Acharya (2007). A ripple-mitigating andenergy-efficient fuel cell power-conditioning system, *IEEE Trans. Power Electron*., vol. 22, no. 4, pp. 1437–1452, Jul. 2007.

XXII. S. Sadaf, N. Al-Emadi, P. K. Maroti and A. Iqbal (2021). A New High Gain Active Switched Network-Based Boost Converter for DC Microgrid Application, *IEEE Access*, vol. 9, pp. 68253-68265. 10.1109/ACCESS.2021.3077055.

XXIII. S. Saha (2021). Soft-switched high step-up DC/DC boost converter for distributed generation, *International Journal of Power Electronics*, vol. 13, no 1, pp. 112-131.

XXIV. Texas instruments (2020). Mitigation procedure on voltage spike of switching node from flyback converter, application report.

XXV. W. Li and X. He (2011). Review of non isolated high-step-up DC/DC converters in photovoltaic grid-connected applications, *IEEE Trans. Ind. Electron.*,vol. 58, no. 4, pp. 12391250.

XXVI. X. Zhu, B. Zhang and K. Jin (2020). Hybrid Nonisolated Active Quasi-Switched DC-DC Converter for High Step-up Voltage Conversion Applications, *IEEE Access*, vol. 8, pp. 222584-222598. 10.1109/ACCESS.2020.3043816.