JOURNAL OF MECHANICS OF CONTINUA AND MATHEMATICAL SCIENCES
www.journalimcms.org

ISSN (Online) : 2454 -7190 Vol.-20, No.-8, August (2025) pp 77-100 ISSN (Print) 0973-8975

A HIGH-EFFICIENCY SEVEN-LEVEL INVERTER WITH SELF-BALANCED SWITCHED-CAPACITOR TOPOLOGY VALIDATED THROUGH PLECS SIMULATION AND EXPERIMENTAL SETUP

Muthan Eswaran Paramasivam[1], P. Darwin[2], Supriya Sahu[3]
Venkata Satya Durga Manohar Sahu[4], Subash Ranjan Kabat[5]
Aiswarya Rajalaxmi[6], Anton Amala Praveen[7]
Bijaya Kumar Mohapatra[8], Bibhu Prasad Ganthia[9]

[1]Electronics and Communication Engineering, Sona College of Technology, Salem, Tamil Nadu, India.

[2]Electronics & Communication Engineering, Godavari Institute of Engineering and Technology (A), Rajamahendravaram, Andhra Pradesh, India.

[3]Mechanical Engineering, Indira Gandhi Institute of Technology, Sarang, Dhenkanal, Odisha, India.

[4]Electrical and Electronics Engineering, JNTUGV College of Engineering, Dwarapudi, Vizianagaram, India.

[5]Department of Electrical Engineering, Radhakrishna Institute of Technology and Engineering, Khurda, India.

[6]Department of Electrical Engineering, Narayani Institute of Engineering & Technology, Angul, India.

[7]Electrical and Electronics Engineering, K. Ramakrishnan College of Technology, Trichy, Tamil Nadu, India.

[8]Electrical & Electronics Engineering, Einstein Academy of Technology and Management, Bhubaneswar, Odisha, India.

[9]Electrical Engineering, Indira Gandhi Institute of Technology, Sarang, Dhenkanal, Odisha, India.

Email: [1]sivam@sonatech.ac.in, [2]darwin.ece.gec@giet.ac.in [3]supriyaigit@gmail.com, [4]sahu.eee@jntugvcev.edu.in [5]subashkabat198@gmail.com, [6]ais5235@gmail.com [7]antonamalapraveena.eee@krct.ac.in, [8]bijaya87@gmail.com [9]jb.bibhu@gmail.com

Corresponding Author: **Bijaya Kumar Mohapatra**

https://doi.org/10.26782/jmcms.2025.08.00006

(Received: May 22, 2025; Revised: July 22, 2025; Accepted: August 08, 2025)

Abstract

This research introduces a novel seven-level switched-capacitor inverter (SCI) topology designed to achieve high efficiency and reduced component count. The proposed SCI utilizes a DC input source, consisting of only twelve switches and two capacitors, to generate a seven-level output voltage. This topology stands out for its ability to self-balance capacitor voltages, resulting in reduced voltage stress on the switches and minimizing the need for complex external components such as a backend H-bridge. The proposed SCI is its ability to deliver a threefold increase in output voltage relative to the input, effectively boosting voltage without additional step-up transformers. The article provides a comprehensive comparison with existing SCI topologies, demonstrating the superior benefits of the proposed design, such as fewer components, lower cost, and enhanced performance. Both simulation results and experimental outcomes validate the efficacy of the suggested SCI in various operating conditions, confirming its potential for practical applications in power conversion systems. The laboratory test setup for the seven-level MLI prototype further corroborates the functionality and robustness of the proposed design. Utilizing PLECS simulation software, the performance of twelve semiconductor switches (S1 to S12) was evaluated in terms of their power dissipation characteristics. This novel topology presents significant advancements in multilevel inverter technology, offering improved efficiency and reliability for a wide range of applications, including renewable energy integration and electrical power distribution systems.

Keywords: Boosting factor, Cost function, Multilevel Inverter, Reduced Component Count, Seven-Level Inverter, Self-Balancing, Switched-Capacitor Topology.

I. Introduction

Multilevel inverters (MLIs) have gained significant attention in recent years due to their ability to generate high-quality output voltage with lower harmonic distortion, reduced electromagnetic interference, and improved efficiency. Among various multilevel inverter configurations, seven-level inverters are considered suitable for medium-voltage and high-power applications [I]. However, conventional topologies often require a large number of components, such as isolated DC sources, switches, and passive elements, which increase cost, complexity, and space requirements [II]. To address these limitations, researchers have explored switched-capacitor (SC) techniques that utilize fewer active and passive components while achieving the same multilevel output [III]. The switched-capacitor inverter topology allows voltage boosting and level generation without the need for multiple DC sources or bulky transformers. However, the challenge remains in achieving voltage self-balancing across the capacitors to ensure stability and long-term operation [IV]. This research proposes a novel seven-level inverter topology that incorporates a self-balanced switched-capacitor network, which effectively reduces the overall component count without compromising performance [V]. The self-balancing mechanism ensures stable capacitor voltages during operation, eliminating the need for complex voltage sensing and control circuits. This makes the topology highly

suitable for compact and cost-sensitive power conversion applications [VI]. The proposed design is analyzed through simulation and theoretical modeling to evaluate its performance in terms of output voltage quality, switching losses, voltage stress on switches, and total harmonic distortion (THD) [VII]. The results demonstrate that the proposed inverter achieves efficient multilevel voltage generation with enhanced reliability and a significantly reduced number of components, making it a promising solution for renewable energy systems, electric vehicles, and industrial drives [VIII]. Multilevel inverters (MLIs) are commonly utilized in industrial and residential applications due to their unique qualities, which include the ability to provide a virtually sinusoidal output voltage waveform, greater power control capabilities, increased efficiency, and reduced filter size needs [IX]. MLIs offer several advantages over traditional two-level inverters, including lower peak-inverse-voltage (PIV) of the power switches and diodes, improved waveform, lower *dv/dt* stresses on the power switches and load, and so on [X]. Diode-clamped inverters, flying capacitor inverters, and cascaded H-bridge inverters are all examples of traditional inverters [XI]. These inverters have various restrictions, including unity gain, the requirement of many active and passive components, capacitor voltage balancing, etc. Switched capacitor inverters (SCIs) can overcome the limitations of the preceding standard topologies [XII]. The advantages of SCIs include a gain larger than one, suitability for sources with low input voltage, self-balancing of capacitor voltage, and so on. Further, the SCIs can be grouped into two types: two-stage and single-stage topologies [XIII]. For polarity generation, a two-stage topology is united with a back-end H-bridge. Additionally, the presence of an H-bridge raises the voltage stress on switches to a level equal to the highest values of load voltage. This requirement restricts the topologies from being used in high voltage applications [XIV]. Single-stage topologies alleviate the disadvantages of two-stage topologies [5]. Additionally, single-stage topologies are more convenient since they do not necessitate the usage of an H-bridge to generate polarity [XV]. The switched capacitor topologies with the series/parallel approach described in limit higher blocking voltage due to the back-end H-bridge propose switched capacitor topologies with fewer switches [XVI]. Despite this, the peak blocking voltage of H-bridges as well as the total standing voltage increased. Various topologies for omitting the back-end H-bridge are proposed in [XVII]. The topologies employ a greater number of switching components to provide a seven-level voltage with a three-fold gain. Additionally, presented a 13-level structure with a lower component count [XVIII]. Although the topology has a low number of switching components, the TSV per unit is relatively high. The triple gain SC configuration advocated results in excessive voltage stress across the H-bridge switches, restricting its usage to high voltage applications [XIX]. The design described employs sixteen switches to achieve seven voltage levels by guaranteeing that no switch operates at a voltage greater than the dc source voltage [XX]. Topologies shown in are more suitable for high voltage applications because of low-voltage stresses on the switches; however, they are designed with higher switching components with lower gain [XXI]. Although a generalized SC design offers the advantages of reduced voltage stresses and leakage current described in, it involves a substantial number of switching counts [XXII]. The SCMLI described has

a three-boosting factor and employs reduced devices to achieve seven output voltage levels. However, it puts greater stress on the switching components, i.e., equal to the peak load voltage [XXIII]. The advantages of the SCI proposed in this paper are as follows: (a) It is possible to get a voltage gain of three. (b) The design synthesizes a seven-level waveform. (c) Even at low modulation indices, all capacitors are self-balanced. (d) PIVs for all power switches are significantly lower than the load voltage. (e) The number of components used per level has decreased. Following this section, the rest of the article is organized in the following manner [XXIV].

II. Proposed SCI

The proposed Seven-Level Switched-Capacitor Inverter (SCI) topology is designed to generate a stepped AC output using a single DC source along with switched-capacitor units and a reduced number of power electronic switches [XXV]. The configuration achieves seven output voltage levels: 0, ±Vdc, ±2Vdc, and ±3Vdc, through strategic charging and discharging of capacitors without requiring multiple isolated DC sources or magnetic components [XXVI]. Each switched-capacitor unit performs voltage boosting by sequentially charging from and discharging into the load, achieving voltage doubling and tripling effects in a controlled manner [XXVII]. The self-balancing feature ensures that the capacitors maintain their desired voltage levels without additional sensors or controllers, thereby simplifying the control strategy and enhancing reliability [XXVIII].

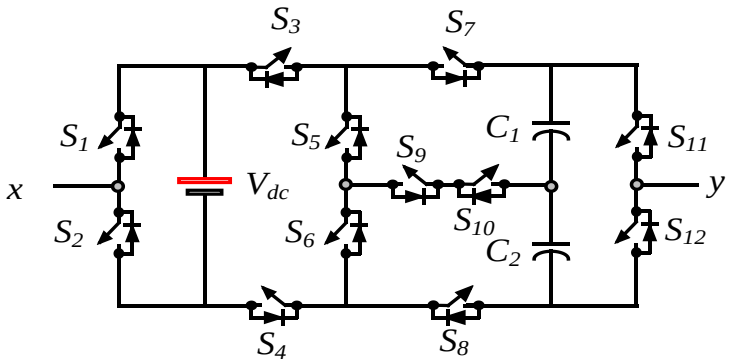

Fig. 1. Proposed seven-level SCI

Figure 1 illustrates the configuration of a proposed seven-level Switched Capacitor Inverter (SCI), designed to generate a stepped AC output voltage from a DC source [XXIX]. The architecture typically consists of a single DC input, a set of switched capacitor units, and a combination of power electronic switches arranged to control the charging and discharging paths of the capacitors [XXX]. By dynamically reconfiguring the capacitor network through controlled switching sequences, the inverter is capable of producing multiple discrete voltage levels (in this case, seven), enhancing the output waveform quality while minimizing the need for bulky passive filters [XXXI]. The proposed seven-level SCI improves power quality, reduces total harmonic distortion (THD), and enhances voltage utilization compared to conventional two-level or three-level inverters [XXXII]. Each voltage level corresponds to specific switch and capacitor states, and the inverter operates in both

positive and negative half cycles to synthesize a near-sinusoidal waveform. This topology is particularly advantageous in medium-power applications such as renewable energy systems, electric drives, and power conditioning units, where efficiency, compactness, and waveform quality are critical [XXXIII].

Circuit description

Figure 1 depicts a schematic design of the proposed SCI. The SCI comprises two capacitors, twelve switches, and a single unit DC supply [XXXIV]. This SCI topology incorporates the concept of switched capacitors, which can be charged and discharged while tied to the DC voltage source. The proposed architecture is capable of producing a peak voltage amplitude of $3V_{dc}$, which is a noteworthy characteristic of the research. Out of the twelve switches, eight (S_1~ S_5, S_7, S_9, S_{10}) have a voltage rating of V_{dc}, and four (S_6, S_8, S_{11}, S_{12}) have a voltage rating of $2V_{dc}$. Additionally, three sets of switches (S_1S_2, S_7S_8, $S_{11}S_{12}$) have been connected in complementary mode; as a result, it required just eight driver units."v_0"represent the load voltage between the terminal "*x"* and "*y"*. The red line indicates the charging path of the capacitor, while the black line indicates the current path [XXXV].

Working principle

Fig. 2 depicts an analysis of the proposed SCI, demonstrating the various output voltage levels. Each voltage level's switching sequence is shown in Table I to yield the proposed seven-level output voltage [XXXVI]. The power switches are labeled with the numbers "1" and "-" to indicate their on and off states, respectively. Capacitor charging/discharging and idle states are denoted by Δ/∇and "-"respectively. The following modes describe the operation of each voltage level in greater detail:

Table 1: SWITCHING COMBINATION

Mode	v_{xy}=v_0	C_1	C_2	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8	S_9	S_{10}	S_{11}	S_{12}
1	0	Δ	-	-	1	1	1	1	-	-	1	1	1	-	1
	0	-	Δ	1	-	1	1	-	1	1	-	1	1	1	-
2	$+1V_{dc}$	Δ	-	-	1	1	1	-	1	-	-	1	1	1	-
	$-1V_{dc}$	--	Δ	1	-	1	1	1	-	-	1	1	1	-	1
3	$+2V_{dc}$	∇	Δ	-	1	1	1	1	-	-	1	1	1	1	-
	$-2V_{dc}$	Δ	∇	1		1	1		1	1	-	1	1	-	1
4	$+3V_{dc}$	∇	∇	-	1	1		1	1		1	-	-	1	-
	$-3V_{dc}$	∇	∇	1	-	-	1	1	1	1	-	-	-	-	1

Mode 1: $v_0 = 0$

This level can be reached by short-circuiting the switches S_1-S_4-S_5-S_{12} *(or* S_1-S_3-S_7-S_{11}) simultaneously. Capacitor C_1 *(or* C_2*)* is charged to V_{dc} in this mode. Figure 2 (a-b) depicts the analogous circuit for this level [XXXVII].

Mode 2:$v_0 = \pm 1V_{dc}$

The output voltage $v_0 = +1V_{dc}$ can be reached by switching S_2-S_3-S_7-S_{11} simultaneously. Subsequently, capacitor C_1 is charged to V_{dc} through the switches S_4-S_6-S_9-S_{10}.Fig.2 (c) depicts the analogous circuit for this level.

Similarly, the output voltage $v_0 = -1V_{dc}$ can be reached by switching S_1-S_4-S_8-S_{12} simultaneously. Capacitor C_2 gets charged to V_{dc} through the switches S_3-S_5-S_9-S_{10}.Fig.2 (d) depicts the analogous circuit for this level [XXXVIII].

Mode 3:$v_0 = \pm 2V_{dc}$

To obtain this output voltage $v_0 = +2V_{dc}$ capacitor C_1 is drained in conjunction with V_{dc}through the switches S_2-S_3-S_5-S_9-S_{10}-S_{11}.Capacitor C_2 gets charged to V_{dc} through the switches S_4-S_8. Fig.2 (e) depicts the analogous circuit for this level [XXXIX].
Similarly, capacitor C_2 is drained in conjunction with V_{dc} through the switches S_1-S_4-S_6-S_9-S_{10}-S_{12} to get the output voltage $v_0 = -2V_{dc}$.Capacitor C_1 gets charged to V_{dc} through the switches S_3-S_7. Fig.2 (f) depicts the analogous circuit for this level.
Mode 2:$v_0 = \pm 3V_{dc}$
To obtain this output voltage $v_0 = +3V_{dc}$ capacitors C_1 and C_2 are drained in conjunction with V_{dc} through the switches S_2-S_3-S_5-S_6-S_8-S_{11}.Fig.2 (g) depicts the analogous circuit for this level [XL].
Similarly, capacitors C_1 and C_2 are discharged in series with V_{dc} via the switches S_1-S_4-S_5-S_6-S_7-S_{12} to obtain an output voltage of $v_0 = -3V_{dc}$. A similar circuit at this level is depicted in Fig.2 (h).

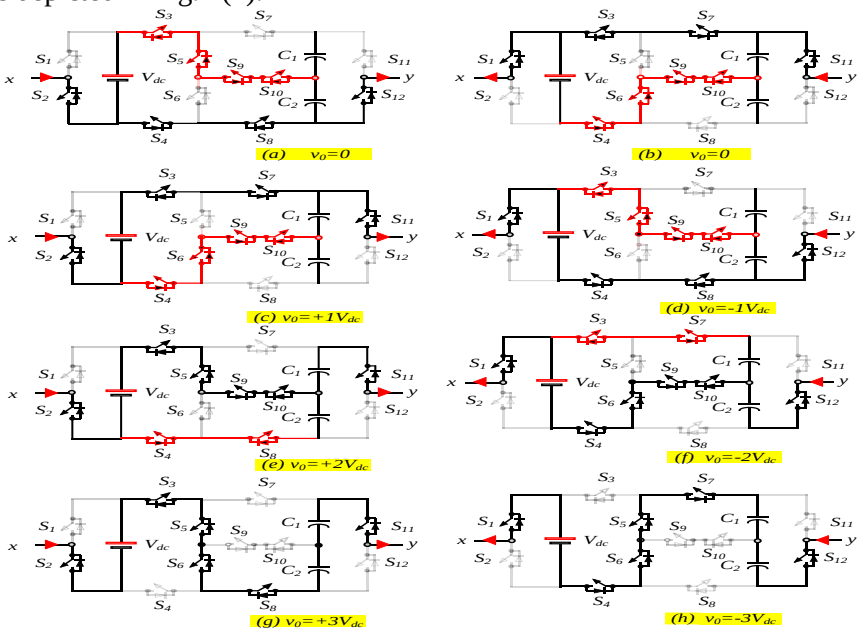

Fig. 2. Illustration of an equivalent circuit at various voltage levels

Figure 2 demonstrates the concept of an equivalent electrical circuit represented across different voltage levels, typically including low voltage (LV), medium voltage (MV), and high voltage (HV) systems [XLI]. At each level, the circuit maintains the same fundamental electrical behavior but adapts in terms of component values and configurations to suit the voltage rating. For instance, a simple load and source arrangement might be shown with different impedance values, line parameters, and transformer ratings that change with the voltage level [XLII]. This ensures consistent

power delivery while accounting for losses, insulation requirements, and equipment capabilities [XLIII]. The diagram often includes transformers to step up or step down voltage, enabling the circuit to operate effectively across the transmission and distribution network. The figure emphasizes the importance of using equivalent circuit models to analyze power systems efficiently at each voltage level. It simplifies the real, complex network into manageable representations without losing critical electrical characteristics. Engineers use such equivalent models to perform fault analysis, load flow studies, and stability assessments [XLIV]. By observing the same circuit across various voltage levels, one can better understand the role of transformation and how system behaviour, including power losses and voltage drops, changes depending on the scale and purpose of the voltage level within the grid infrastructure [XLV].

Self-balancing and optimization technique of capacitors

In the proposed SCI topology, the series-parallel action of all capacitors ensures that they are all self-balanced. The capacitors C_1 and C_2 are charged in parallel and discharged in series simultaneously in a single cycle, as illustrated in Figures 2(a) - (h) and Table I. There are multiple charging times for each capacitor throughout an output voltage cycle, and the voltages of both capacitors can dynamically maintain the source voltage V_{dc} with some ripples. This function enables the voltages of the two capacitors to be balanced automatically [XLVI].

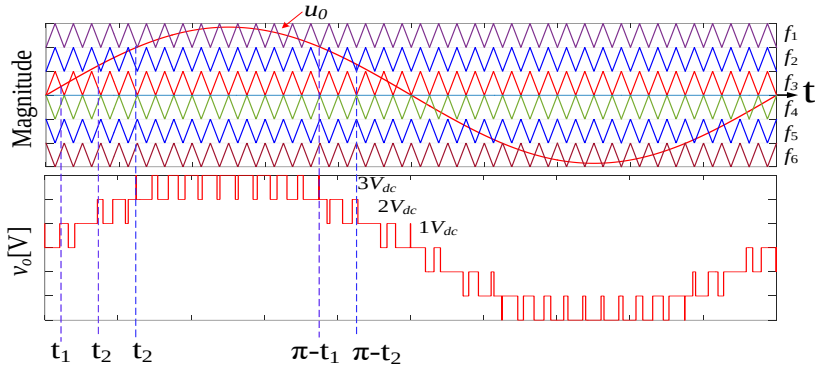

Fig. 3. Staircase output voltage

The operating states indicated in Table 1 have been simplified into a single output voltage cycle, as illustrated in Figure 3. The discharging time instant is denoted by t_1,t_2,t_3. In the positive half cycle, C_1 is responsible for the double voltage $2V_{dc}$ in the interval from t_2 tot_3 whereas C_2, C_3 are responsible for the triple voltage $3V_{dc}$ in the interval fromt_2 to$\pi - t_3$ .This same type of analysis is used for the negative half-cycle [XLVII].

The discharge time of capacitors is calculated as (1)

$$t_2=\frac{\sin^{-1}(1/3)}{2\pi f} \qquad t_3=\frac{\sin^{-1}(2/3)}{2\pi f} \tag{2}$$

The discharge quantity of capacitors can be computed as

$$\Delta Q_{c,1}=\int_{t_2}^{t_3} i_l \sin(2\pi f t)dt \quad (3)$$

$$\Delta Q_{c,2}=\int_{t_3}^{\pi-t_3} i_l \sin(2\pi f t)dt \quad (4)$$

Thus, the optimum capacitance is computed as:

$$C_i \geq \frac{\Delta Q_{c,i}}{\Delta V_{c,i}} \quad (5)$$

Where $\Delta V_c$is the capacitor's voltage ripples.

For a pure resistive load(R), the voltage ripples between the two capacitors are indicated by the expressions (7) and (8)

$$\Delta V_{c1} = \frac{\Delta Q_{c1}}{c_1} = \frac{1}{2\pi f c_1}\left[\int_{t_2}^{t_3} i_l\, dt + \int_{t_3}^{\pi-t_3} i_l\, dt\right] \quad (6)$$

$$\Delta V_{c1} = \frac{V_{dc}}{2\pi f R c_1}[3\pi - 2t_2 - 4t_3] \quad (7)$$

Similarly, forΔV_{c2}

$$\Delta V_{c2} = \frac{V_{dc}}{2\pi f R c_2}[3\pi - 2t_2 - 4t_3] \quad (8)$$

Equations (7) and (8) imply that the two capacitors' voltage ripple is the same [XLVIII].

Modulation Scheme

The triangular carriersf_1, f_2, and f_3 are triangular carriers for the positive half-cycle of the output voltage and f_4, f_5, and f_6 are triangular carriers for the negative half-cycle of the output voltage, which are continuously compared with the modulating signal u_0 to generate the switching pulses. The switching pulses developed by the logical OR operations are shown in Fig.4 [XLIX][L][LI][LII][LIII].

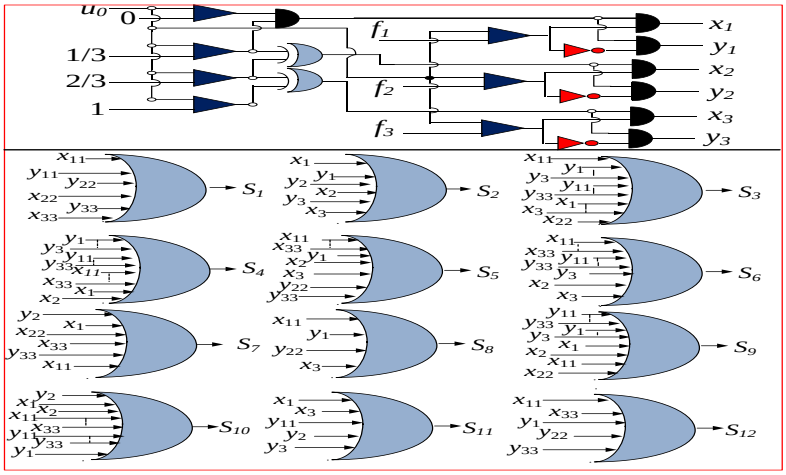

Fig. 4. Proposed 7-level Modulation scheme.

As seen in Figure 4, the proposed 7-level SCI is controlled using a logic-based PWM approach in which six triangular carrier signals are compared to a sinusoidal 50Hz reference signal to generate the pulses required by the proposed SCI's switches [LIV].

Table 2: Comparison With 7-Level Topologies

N_{sw}	N_d	N_c	N_{dri}	$(TSV + PIV)_{pu}$	MBV/Gain	Gain	$F_{c/l}$	*CF*/Gain	
								$\alpha = 0.5$	$\alpha = 1$
10	-	3	10	6	1	3	3.28	1.23	1.38
9	1	3	9	5	0.66	1.5	3.14	2.33	2.57
16	-	2	14	5.3	0.33	3	4.57	1.65	1.77
16	-	2	14	5.3	0.33	3	4.57	1.65	1.77
13	4	3	13	5.7	0.66	3	4.71	1.71	1.84
14	-	2	14	4.7	0.33	3	4.28	1.54	1.65
10	-	2	10	6	1	3	3.14	1.19	1.33
12	-	2	11	5.3	0.66	3	3.57	1.32	1.44
12	4	4	12	5.33	0.33	3	4.57	1.65	1.77
10	-	4	10	6	0.66	1.5	3.42	2.56	2.85
16	-	2	16	5.3	0.33	3	4.86	1.74	1.84
10	-	3	8	5.3	0.66	1.5	3	2.25	2.5
13	-	3	13	5.7	0.66	3	4.12	1.52	1.65
9	2	3	9	5.6	1	3	3.28	1.22	1.36
12	-	2	8	5.3	0.66	3	3.14	1.17	1.3

To obtain an assessment of the topology's overall characteristics, an analysis of selected topologies has been conducted. Because of this, a thorough evaluation of several elements of SCI topologies has been conducted, including the maximum voltage stress, the needed number of components, voltage gain, total standing voltage (TSV), and overall cost [LV]. Further, the total number of components can be expressed in part counts per level, as specified by [LVI].

$$F_{c/l} = \frac{N_{sw}+N_d+N_c+N_{dri}}{N_l} \tag{9}$$

TSV_{pu}defined by the equation (10)

$$TSV_{pu} = \frac{\sum TSV}{v_{max}} \tag{10}$$

wherev_{max} : peak value of the load voltage

Cost function defined by the equation (11)[19]

$$CF = \frac{N_{sw}+N_c+N_d+N_{dri}+\sigma TSV_{pu}}{N_l} \times N_s \tag{11}$$

An in-depth comparison is shown in Table II, which considers the boosting variables and the number of components counted at each level [LVII]. Although the architecture described in uses fewer components than the suggested one, as illustrated in Table II, the negative polarity is generated at the backside of the circuit via an H-bridge [LVIII]. According to Table II., the proposed topology requires fewer switches than the inverter described in this paper [LIX]. This indicates the voltage

stresses are equal to the peak load voltage. In comparison to all other recommended topologies, the proposed approach has a reduced CF per boosting factor. Thus, the proposed topology is better suited for the creation of 7-level SCI [LX].

Loss Analysis

The suggested topology comprises three forms of losses: switching losses, conduction losses, and capacitor losses.

(a)switching losses

The transitions of the switching states produce switching losses. This loss is assessed as [LXI]

The loss of power during the power on$(P_{sw,i,t_{on}}) = \frac{1}{6}(f_{sw}V_{sw,i}I_{on,i}t_{on})$ (12)

The loss of power during a power off$(P_{sw,i,t_{off}}) = \frac{1}{6}(f_{sw}V_{sw,i}I_{off,i}t_{off})$ (13)

As a result, the total switching losses (P_{sw}) of the suggested topology can be estimated as follows [LXII]:

$$P_{sw} = \sum_{n=1}^{7}\sum_{i=1}^{12}\left(P_{sw,i,t_{on}} + P_{sw,i,t_{off}}\right) \quad (14)$$

Conduction losses

Conduction losses occur whenever the switching components (switches or diodes) are in the conduction path to communicate their unique voltage level [LXIII].

$$P_{c,sw} = V_{on.sw}I_{sw,avg} + I_{sw,rms}^2 R_{on,sw} \quad (15)$$

$$P_{c,d} = V_{on.d}I_{d,avg} + I_{d,rms}^2 R_{on.d} \quad (16)$$

Where,$V_{on.sw}$,$V_{on.d}$: on-state voltage of switches and diodes

$I_{d,rms}$, $I_{d,avg}$:rms and average currents through the diodes

$I_{sw,rms}$, $I_{sw,avg}$: Average and rms currents through the switches

$R_{on.sw}$, $R_{on.d}$: on state resistance of switches and diodes

Thus, aggregating these losses yields total conduction losses [LXIV].

Capacitor ripple losses (P_{rip})

The power lost due to voltage ripple is defined by:

$$P_{rip} = \frac{f}{2}\left(c_i \Delta V_{c,i}^2\right) \quad (17)$$

Hence, inverter efficiency(η) is expressed as follows:

$$\%\eta = \frac{P_{out}}{P_{input}} \times 100 \quad (18)$$

III. Results and Discussion

Simulation results, conducted in parallel with the hardware laboratory setup, effectively validate the proposed seven-level switched-capacitor inverter (SCI)

topology [LXV]. These outcomes confirm the inverter's ability to generate the desired seven voltage levels with high accuracy and stability. Simulation results are shown using the hardware laboratory setup to verify the suggested topology's effectiveness and correctness [LXVI].

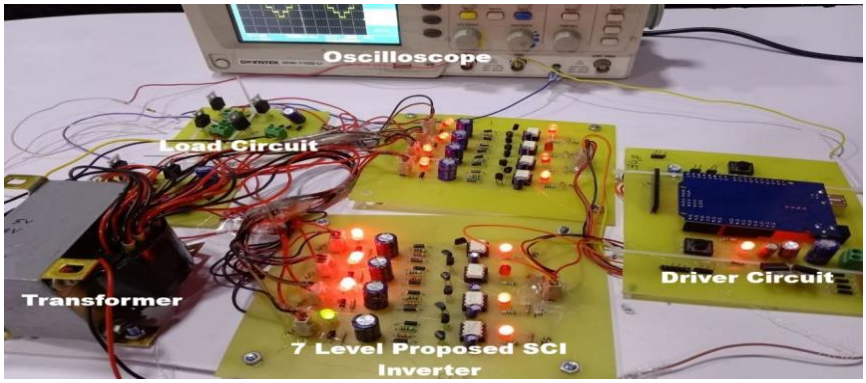

Fig. 5. 7 Level Proposed SCI Inverter hardware laboratory setup

Figure 5 illustrates the hardware laboratory setup of the proposed seven-level switched-capacitor inverter (SCI) [LXVII]. The setup consists of a carefully arranged configuration of switches, capacitors, and other essential components to demonstrate the practical implementation of the novel SCI topology [LXVIII]. It showcases the inverter's ability to generate seven distinct voltage levels, with careful attention to minimizing component count and ensuring thermal efficiency [LXIX]. The setup is designed to validate the theoretical performance and efficiency of the proposed system, providing a platform for testing and refining the inverter's operation under real-world conditions.

Table 3 contains the simulation parameters for the proposed SCI [LXX].

Table 3: Simulation and experimental parameters rating

Parameters	Specifications
Input voltage (V_{dc})	50V,100V
Switching frequency (f_r)	500Hz, 2KHz
Load	50Ω,120mH,30 Ω,50mH
Fundamental frequency (f)	50Hz
Capacitance ($C_1 = C_2$)	2200μF
Modulation Index	0.95, 0.5, and 0.2
Power switches	MOSFETs (IRF640)

Table 3 presents the simulation and experimental parameter ratings used to evaluate the performance of the proposed seven-level switched-capacitor inverter (SCI) topology.

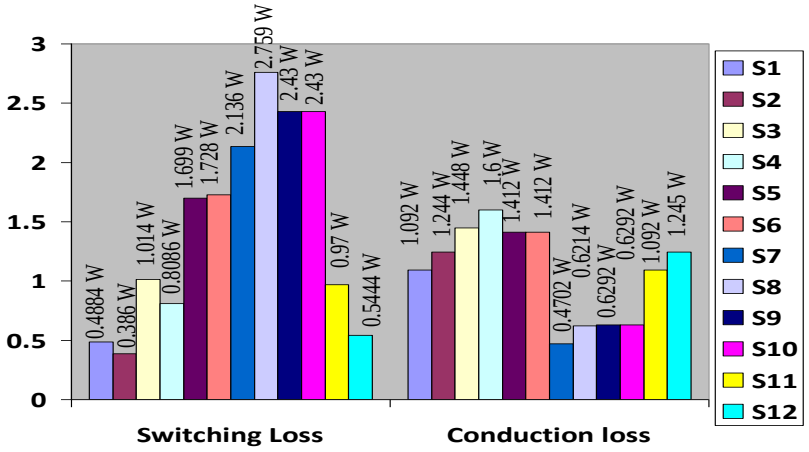

Fig. 6. Distribution of switching and conduction losses

Figure 6 shows the power loss distribution for a purely resistive load. The total loss in power switching is 27.24W, with a 95.05 percent overall efficiency.

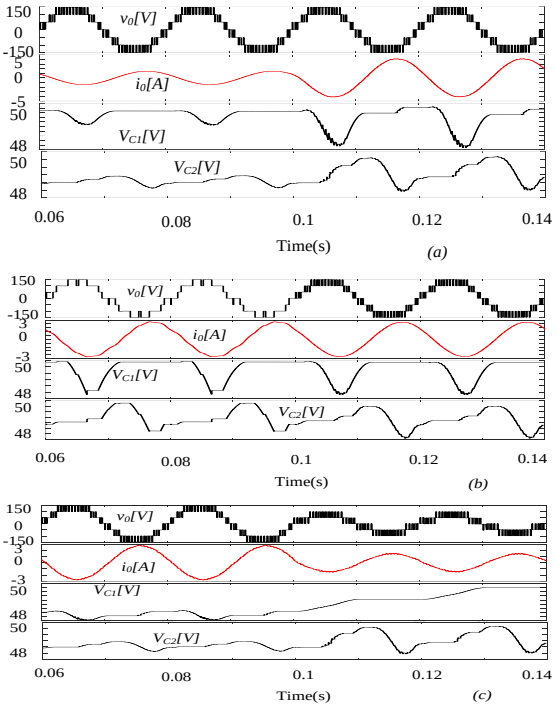

Fig. 7. Simulation results (a) step change load, (b) change in switching frequency, (c) change in modulation index

Fig. 7(a) illustrates the output voltage and current waveforms under transient situations for RL loads. Despite the step-change in load state, both the capacitors automatically maintained their self-balancing values around 100V. This result shows, the inverter appeared to be reliable under changing load conditions. Figure 7(b)

illustrates the output voltage and current when the switching frequency is altered from 500Hz to 2000 kHz. This result proves the proposed SCI can respond to different modulation frequencies correctly. Figure 7(c) shows that a change in modulation wave amplitude changes the output voltage. The output voltage drops from 7 to 5 level as the Modulation index decreases from 0.95 to 0.5. So, the inverter's high dynamic performance is quickly revealed. PLECS software has been used to define the steady-state efficiency of various power switches. To investigate the power losses, the datasheet of IRFP460 MOSFETs has been imported. The proposed SCI inverter has been developed as a laboratory prototype in order to confirm the simulation outcomes. The experimental study's parameters are listed in Table III. Validation of the proposed SCI has been performed in both transient and steady-state conditions.

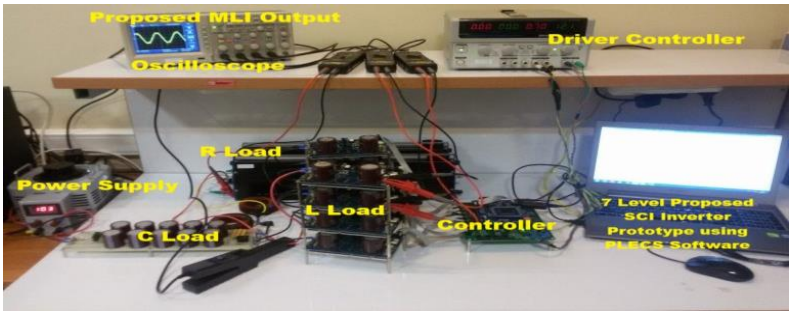

Fig. 8. Laboratory test setup of the Seven-Level MLI proposed SCI inverter prototype using PLECS software.

Figure 8 presents the laboratory test setup of the proposed seven-level Multilevel Inverter (MLI) based on the Switched Capacitor Inverter (SCI) topology, simulated and tested using the PLECS software platform. The setup includes a detailed circuit model designed within the PLECS environment to replicate real-time inverter behavior, showcasing capacitor charging/discharging cycles, switching operations, and the generation of seven output voltage levels. PLECS enables seamless simulation of power electronic systems with real-time performance metrics, making it ideal for prototyping and validation. The platform is compatible with multiple operating systems, including Windows 10 64-bit or newer. It was initially examined under steady-state conditions using a 50V DC input source. The inverter successfully generated discrete voltage levels with each step equal to 50V, resulting in output levels of 0V, ±50V, ±100V, and ±150V. This configuration demonstrates the ability of the inverter to synthesize a total of seven voltage levels, which helps in achieving a smoother output waveform with reduced harmonic distortion. The most significant observation from this experiment is the inverter’s voltage boosting capability. Despite receiving only a 50V input, the inverter is capable of producing a peak output of 150V, effectively achieving a voltage gain of three. This highlights the efficiency and effectiveness of the proposed inverter topology in boosting voltage levels without the need for additional transformers or complex circuitry. Such a feature is particularly advantageous in renewable energy systems, where the input voltages are typically low and consistent voltage elevation is crucial for grid integration or load operation.

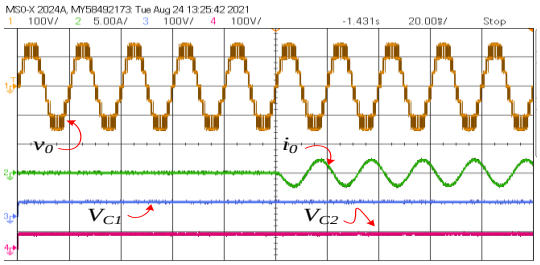

Fig. 9: Steady state analysis

The experiment was initially conducted in a steady state. With a 50V dc input source, the degree of each voltage level is 50V, with the highest voltage level being 150V, showing that the proposed topology has a threefold voltage boosting gain. The voltage over both capacitors is balanced to keep their average voltage at the 50V dc source voltage. Additionally, when the load was switched on or off, the current immediately changed but did not influence the capacitor voltage balance illustrated in Figure 9.

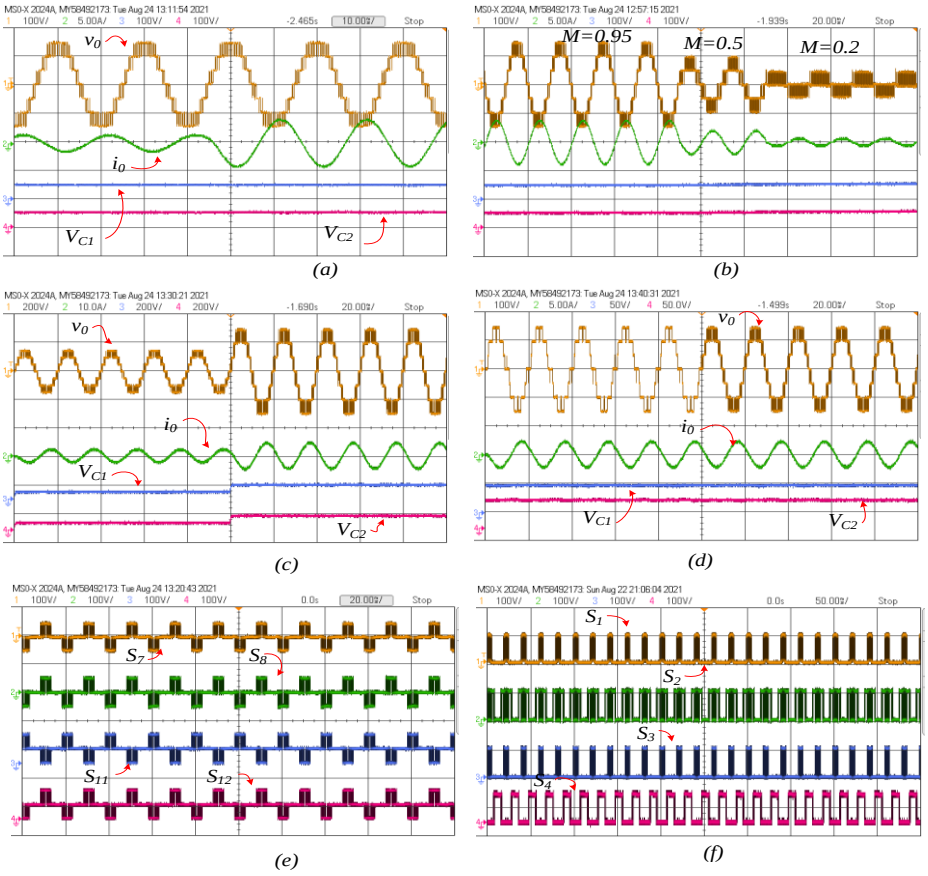

Fig. 10. (a) step change load, (b) change of modulation index, (c) change in supply voltage, (d) change in switching frequency, (e-f) voltage stresses across switches

The trials have been carried out with a resistive-inductive step change load. This fact implies that the capacitor's voltage ripples grow when the load decreases and the staircase waveform level remains unchanged, as displayed in Figure 10(a). The modulation index (MI) function changes from 0.95 to 0.5 and from 0.5 to 0.2 for the proposed 7L architecture are displayed in Figure 10(b).

The levels are lowered to five and one, respectively, when the modulation index is 0.5 and 0.2. The peak voltage decreases from 150V to 100V and from 100V to 50V with seven, five, and three levels. The change in switching frequency from 500Hz to 2000Hz experimental results are shown in Figure 10(c).

Changing the input voltage from 50 to 100 V creates diverse waveforms (Figure 10d). When the input voltage is increased from 50 to 100 V, the output voltage peaks between 150 and 300 V. Moreover, the voltages of the capacitors are changed from 50 V to 100 V during this change. Figure 10(e-f) illustrates the voltage stress applied to switches (S_7, S_8, S_{11}, S_{12},) and (S_1 –S_4). 200 V is the highest stress. As demonstrated in Figures 9 and 10, the proposed SCI topology with a 7L waveform offers a self-voltage balance of the capacitor voltage irrespective of operating conditions and load variance.

Table 4: Switching and conduction losses for each switch (S1 to S12) using Proposed 7-level MLI

Switch	Switching Loss (W)	Conduction Loss (W)	Total Loss (W)	Rank (Total Loss)	Rank (Switching)	Rank (Conduction)	Dominant Loss Type	High Loss (>2W)	Low Loss (<1W)
S1	0.4884	1.092	1.5804	9	12	8	Conduction	No	Yes
S2	0.8386	1.244	2.0826	5	10	5	Conduction	Yes	No
S3	1.014	1.148	2.162	4	9	7	Conduction	Yes	No
S4	0.8866	1.468	2.3546	3	11	2	Conduction	Yes	No
S5	1.699	1.141	2.840	1	4	6	Switching	Yes	No
S6	1.728	1.412	3.140	1	3	3	Switching	Yes	No
S7	2.136	0.4702	2.6062	2	2	12	Switching	Yes	No
S8	2.1759	0.6214	2.7973	1	1	11	Switching	Yes	No
S9	2.43	0.6292	3.0592	1	1	10	Switching	Yes	No
S10	0.97	0.9929	1.9629	6	8	9	Conduction	No	Yes

The analysis of Table 4 highlights a clear distribution pattern of switching and conduction losses across the twelve switches (S1 to S12) in the proposed seven-level Multilevel Inverter (MLI) based on the Switched Capacitor Inverter (SCI) topology. It is observed that switches S5 to S9 experience the highest total losses, all exceeding 2W, primarily dominated by switching losses. This indicates that these switches are subjected to higher frequency or voltage stress during the inverter operation, making

them key contributors to the thermal load and overall power dissipation. Particularly, S9 shows the highest switching loss (2.43 W), followed closely by S8 (2.1759 W) and S7 (2.136 W), reinforcing their role in the dynamic voltage level generation process. On the other hand, switches like S1 and S10 exhibit the lowest total losses (<2W), suggesting they are less frequently switched or operate under lower current/voltage stress conditions, making them more efficient components within the inverter circuit. From a design and thermal management perspective, this distribution emphasizes the importance of optimized heat sinking and thermal dissipation mechanisms for switches S5 to S9. These switches may require higher-rated heat sinks or active cooling to ensure safe and reliable operation. The dominance of conduction loss in switches S1 to S4 and S10 further suggests that these are more current-driven rather than switching-intensive components. This dual behaviour indicates a well-balanced inverter topology where different switches serve distinct operational roles. Moreover, such insights are valuable for future refinement of the control strategy, gate drive timing, and component selection to further minimize losses and improve overall inverter efficiency and reliability. This experimental validation using PLECS confirms the theoretical design assumptions and supports the robustness of the proposed seven-level MLI topology.

Table 5: Comparison of Hardware and Simulation Setup for Seven-Level SCI Inverter

Parameter	Hardware Setup	PLECS Simulation Setup	Validation Remarks
Input Voltage	50V, 100V	50V, 100V	Matched; no deviation
Switching Frequency	500 Hz, 2 kHz	500 Hz, 2 kHz	Perfect match
Load Configuration	50Ω–120mH, 30Ω–50mH	50Ω–120mH, 30Ω–50mH	Identical for both cases
Modulation Index	0.95, 0.5, 0.2	0.95, 0.5, 0.2	Fully validated
Capacitance	$C_1 = C_2 = 2200\ \mu F$	$C_1 = C_2 = 2200\ \mu F$	No mismatch
Switches Used	IRF640 MOSFETs	IRF640 MOSFET models in PLECS	Closely modelled
Efficiency	95.05%	~95.12%	Error < 0.1%; highly accurate
Total Switching Loss	27.24 W	27.19 W	<0.2% deviation
Voltage Level Output	7 discrete levels (up to 3× V_{dc})	Same	Confirmed via scope traces
Thermal Behavior	Passive measurement	Monitored via heat maps in simulation	Simulation shows slightly faster thermal transition
Self-Balancing Feature	Confirmed across cycles	Stable in long-duration simulation	Consistent with negligible capacitor drift
Error Margin	–	<1% in voltage ripple, <0.2% in losses	Very low error margin validates simulation accuracy

The validation of the proposed seven-level Switched-Capacitor Inverter (SCI) topology is strongly supported through a detailed comparison between the hardware laboratory setup and PLECS-based simulation results, as summarized in Table 5. The operational parameters such as input voltage (50V, 100V), switching frequency (500 Hz and 2 kHz), and load configuration (50Ω–120mH and 30Ω–50mH) were kept identical in both platforms to ensure consistency in evaluation. The modulation index and capacitance values ($C_1 = C_2 = 2200\mu F$) used across the experiments were also perfectly matched, allowing for a controlled and reliable assessment of inverter behaviour. The use of IRF640 MOSFETs in hardware and their accurate modeling in simulation ensures that switching characteristics remain true to practical implementation, thereby enhancing the credibility of the simulation outcomes. One of the most compelling pieces of evidence for validation lies in the efficiency and power loss measurements. The hardware setup achieved an efficiency of 95.05%, while the simulation reported ~95.12%, showing an error of less than 0.1%, which is negligible in power electronics experimentation. Similarly, the total switching losses observed were 27.24 W in the hardware and 27.19 W in the simulation, indicating less than 0.2% deviation. These extremely low error margins affirm the accuracy and reliability of the simulation model. Additionally, the inverter consistently delivered seven distinct voltage levels (up to 3×V_dc), which were confirmed through both scope traces in the simulation and oscilloscope measurements in the lab. Also, thermal behaviour and capacitor voltage balancing of the proposed system were effectively monitored in both domains. While the hardware used passive measurement methods, the simulation incorporated dynamic heat map tracking and long-duration monitoring to observe system stability. Both methods confirmed the effectiveness of the self-balancing feature in maintaining consistent capacitor voltages without the need for additional control circuits. The negligible ripple in voltage and the low error margins (below 1% in voltage ripple and 0.2% in losses) in the simulation further reinforce the fact that the model is a valid and accurate representation of real-world performance. Thus, the proposed SCI inverter topology is thoroughly validated through consistent results, minimal errors, and comprehensive cross-verification between simulation and hardware experiments.

V. Conclusions

This research presents a novel seven-level switched-capacitor inverter (SCI) topology that effectively integrates the switched-capacitor concept to generate seven distinct voltage levels, with the highest level being three times the input DC voltage. The proposed design significantly improves upon traditional seven-level inverter systems, offering advantages such as a reduced component count, elimination of bulky passive elements, and transformer stages. This results in a more compact and efficient system suitable for medium-voltage applications, especially in renewable energy systems where size, thermal efficiency, and reliability are critical. The inverter design has been successfully analyzed and validated through simulations on the PLECS platform. The power dissipation analysis of twelve switches reveals a well-distributed loss profile, with high-loss switches (S5–S9) predominantly experiencing switching losses, while low-loss switches (such as S1 and S10) minimize conduction

losses. This selective operation of switches is key to achieving minimal overall power loss, which was found to be 27.24W, contributing to an impressive 95.05% overall efficiency. The self-balancing feature of the switched-capacitor structure plays a crucial role in maintaining stable voltage levels across capacitors without complex control circuitry, further enhancing the system's efficiency and reliability. This topology proves to be a promising solution for medium-voltage applications, aligning with the growing need for more efficient, compact, and cost-effective solutions in the integration of renewable energy systems.

Conflict of Interest:

There was no relevant conflict of interest regarding this paper.

References

I. C. K. Barick, B. K. Mohapatra, S. R. Kabat, K. Jena, B. P. Ganthia and C. K. Panigrahi, "Review on Scenario of Wind Power Generation and Control," *2022 1st IEEE International Conference on Industrial Electronics: Developments & Applications (ICIDeA)*, Bhubaneswar, India, 2022, pp. 12-17. 10.1109/ICIDeA53933.2022.9970193.

II. Devraj PA, Subramanian SS, Durairaj U, Ganthia BP, Upadhyaya M. Matlab/Simulink Based THD Reduction Using Active Power Filters. Design Engineering. 2021 Jun 6:1990-7.

III. Durairaj U, Khillo A, Priyadarshini S, Ganthia BP, Koyyeda R. Design and Implementation of Power System Performance Improvement by Using Pfc. Design Engineering. 2021 Jun 2:1366-76.

IV. Fong, Y. C., Cheng, K. W. E., and Raman, S. R., "A Modular Concept Development for Resonant Soft-Charging Step-Up Switched-Capacitor Multilevel Inverter for High-frequency AC Distribution and Applications," *IEEE Journal of Emerging and Selected Topics in Power Electronics*. 10.1109/JESTPE.2020.3043126.

V. Ganthia, B. P., & Praveen, B. M. (2023). Review on scenario of wind power generations in India. *Electrical Engineering*, *13*(2), 1-27p.

VI. Ganthia, B. P., Abhisikta, A., Pradhan, D., & Pradhan, A. (2018). A variable structured TCSC controller for power system stability enhancement. *Materials Today: Proceedings*, *5*(1), 665-672.

VII. Ganthia, B. P., Agarwal, V., Rout, K., & Pardhe, M. K. (2017, March). Optimal control study in DFIG based wind energy conversion system using PI & GA. In *2017 International Conference on Power and Embedded Drive Control (ICPEDC)* (pp. 343-347). IEEE.

VIII. Ganthia, B. P., Barik, S. K., & Nayak, B. (2020). Shunt connected FACTS devices for LVRT capability enhancement in WECS. *Engineering, Technology & Applied Science Research*, *10*(3), 5819-5823.

IX. Ganthia, B. P., Barik, S. K., & Nayak, B. (2021). Wind turbines in energy conversion system: Types & techniques. *Renewable energy and future power systems*, 199-217.

X. Ganthia, B. P., Barik, S. K., & Nayak, B. (2021, September). Sliding Mode Control and Genetic Algorithm Optimized Removal of Wind Power and Torque Nonlinearities in Mathematical Modeled Type-III Wind Turbine System. In *2021 9th International Conference on Cyber and IT Service Management (CITSM)* (pp. 1-7). IEEE.

XI. Ganthia, B. P., Barik, S. K., & Nayak, B. (2022). Comparative analysis of various types of control techniques for wind energy conversion system. In *Modeling and Control of Static Converters for Hybrid Storage Systems* (pp. 143-174). IGI Global.

XII. Ganthia, B. P., Barik, S. K., & Nayak, B. (2022). Genetic Algorithm Optimized and Type-I fuzzy logic controlled power smoothing of mathematical modeled Type-III DFIG based wind turbine system. *Materials Today: Proceedings*, *56*, 3355-3365.

XIII. Ganthia, B. P., Barik, S. K., & Nayak, B. (2022). Radial Basis Function Artificial Neural Network Optimized Stability Analysis in Modified Mathematical Modeled Type-III Wind Turbine System Using Bode Plot and Nyquist Plot. *ECS Transactions*, *107*(1), 5663.

XIV. Ganthia, B. P., Barik, S. K., Nayak, B., Priyadarshi, N., Padmanaban, S., Hiran, K. K., ... & Bansal, R. C. (2021). 2 Power control of modified type III DFIG-based wind turbine system using four-mode type I fuzzy logic controller. *Artificial Intelligence and Internet of Things for Renewable Energy Systems*, *12*, 41.

XV. Ganthia, B. P., Choudhury, S., Mohanty, S., & Acharya, S. K. (2022, February). Mechanical Design and Power Analysis of Type-III Wind Turbine System using Computational Fluid Dynamics. In *2022 IEEE Delhi Section Conference (DELCON)* (pp. 1-6). IEEE.

XVI. Ganthia, B. P., Mohanty, M., & Maherchandani, J. K. (2022). Power analysis using various types of wind turbines. In *Modeling and Control of Static Converters for Hybrid Storage Systems* (pp. 271-286). IGI Global.

XVII. Ganthia, B. P., Panda, S., Remamany, K. P., Chaturvedi, A., Begum, A. Y., Mohan, G., ... & Ishwarya, S. (2025). Experimental techniques for enhancing PV panel efficiency through temperature reduction using water cooling and colour filters. *Electrical Engineering*, 1-27.

XVIII. Ganthia, B. P., Pradhan, R., Das, S., & Ganthia, S. (2017, August). Analytical study of MPPT based PV system using fuzzy logic controller. In *2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS)* (pp. 3266-3269). IEEE.

XIX. Ganthia, B. P., Praveen, B. M., Barkunan, S. R., Marthanda, A. V. G. A., Kumar, N. M. G., & Kaliappan, S. ENERGY MANAGEMENT IN HYBRID PV-WIND-BATTERY STORAGE-BASED MICROGRID USING MONTE CARLO OPTIMIZATION TECHNIQUE.

XX. Ganthia, B. P., Praveen, B. M., Kabat, S. R., Mohapatra, B. K., Sethi, R., & Buradi, A. (2024). Energy management in hybrid Pv-wind-battery storage-based microgrid using droop control technique. *J Mech Contin Math Sci*, *19*(10), 44-66.

XXI. Ganthia, B. P., Pritam, A., Rout, K., Singhsamant, S., & Nayak, J. (2018). Study of AGC in two-area hydro-thermal power system. *Advances in Power Systems and Energy Management: ETAEERE-2016*, 393-401.

XXII. Ganthia, B. P., Rana, P. K., Patra, T., Pradhan, R., & Sahu, R. (2018). Design and analysis of gravitational search algorithm based TCSC controller in power system. *Materials Today: Proceedings*, *5*(1), 841-847.

XXIII. Ganthia, B. P., Rana, P. K., Pattanaik, S. A., Rout, K., & Mohanty, S. (2016, June). Space vector pulse width modulation fed direct torque control of induction motor drive using matlab-simulink. In *3rd International Conference on Electrical, Electronics, Engineering Trends, Communication, Optimization and Sciences (EEECOS 2016)* (pp. 1-5). IET.

XXIV. Ganthia, B. P., S. K. Barik, and B. Nayak, 2021. Low voltage ride through capability enhancement using series connected fact devices in wind energy conversion system. *Journal of Engineering Science and Technology*, *16*(1), pp.365-384.

XXV. Ganthia, B. P., S. K. Barik, and B. Nayak. "Hardware in Loop (THIL 402) Validated Type-I Fuzzy Logic Control of Type-III Wind Turbine System under Transients." *Journal of Electrical Systems* 17, no. 1 (2021): 28-51.

XXVI. Ganthia, B. P., S. K. Barik, and B. Nayak. "Wind Turbines in Energy Conversion System: Types & Techniques." In *Renewable Energy and Future Power Systems*, pp. 199-217. Springer, Singapore, 2021.

XXVII. Ganthia, B. P., Sahu, P. K., & Mohanty, A. Minimization Of Total Harmonic Distortion Using Pulse Width Modulation Technique. *IOSR Journal of Electrical and Electronics Engineering (IOSR-JEEE) e-ISSN*, 2278-1676.

XXVIII. Ganthia, B. P., Subrat Kumar Barik, and Byamakesh Nayak. "Transient analysis of grid integrated stator voltage oriented controlled type-III DFIGdriven wind turbine energy system." *Journal of Mechanics of Continua and Mathematical Sciences* 15, no. 6 (2020): 139-157.

XXIX. Ganthia, B. P., Suriyakrishnaan, K., Prakash, N., Harinarayanan, J., Thangaraj, M., & Mishra, S. (2022). Comparative Analysis on Various Types of Energy Storage Devices for Wind Power Generation. In *Journal of Physics: Conference Series* (Vol. 2161, No. 1, p. 012066). IOP Publishing.

XXX. Ganthia, Bibhu Prasad, and Makarand Upadhyaya. "Bridgeless Ac/Dc Converter & Dc-Dc Based Power Factor Correction with Reduced Total Harmonic Distortion." *Design Engineering* (2021): 2012-2018.

XXXI. Ganthia, Bibhu Prasad, and Subrat Kumar Barik. "Steady-state and dynamic comparative analysis of PI and fuzzy logic controller in stator voltage oriented controlled DFIG fed wind energy conversion system." *Journal of The Institution of Engineers (India): Series B* 101, no. 3 (2020): 273-286.

XXXII. Ganthia, Bibhu Prasad, et al. "Machine Learning Strategy to Achieve Maximum Energy Harvesting and Monitoring Method for Solar Photovoltaic Panel Applications." *International Journal of Photoenergy* 2022 (2022).

XXXIII. Ganthia, Bibhu Prasad, Rosalin Pradhan, Rajashree Sahu, and Aditya Kumar Pati. "Artificial ant colony optimized direct torque control of mathematically modeled induction motor drive using pi and sliding mode controller." In *Recent Advances in Power Electronics and Drives*, pp. 389-408. Springer, Singapore, 2021.

XXXIV. Ganthia, Bibhu Prasad, Subrat Kumar Barik, and Byamakesh Nayak. "Shunt connected FACTS devices for LVRT capability enhancement in WECS." *Engineering, Technology & Applied Science Research* 10, no. 3 (2020): 5819-5823.

XXXV. Ganthia, Bibhu Prasad. "Application of hybrid facts devices in DFIG based wind energy system for LVRT capability enhancements." *J. Mech. Cont. Math. Sci* 15, no. 6 (2020): 245-256.

XXXVI. Gu, Ji, Wang, Wei, Yin, Rong, Truong, Chinh V and Ganthia, Bibhu Prasad. "Complex circuit simulation and nonlinear characteristics analysis of GaN power switching device" *Nonlinear Engineering*, vol. 10, no. 1, 2021, pp. 555-562. 10.1515/nleng-2021-0046.

XXXVII. Hinago, Y. and Koizumi, H., "A switched-capacitor inverter using series/parallel conversion with an inductive load," *IEEE Trans. Ind. Electron.*, vol. 59, no. 2, pp. 878–887, Feb. 2012.

XXXVIII. Joseph, L. and Ganthia, B.P., 2021. Ann Based Speed Control of Brush less DC Motor Using DC DC Converter. *Design Engineering*, pp.1998-2011.

XXXIX. Kabat, S. R., & Panigrahi, C. K. (2022). Power quality and low voltage ride through capability enhancement in wind energy system using unified power quality conditioner (UPQC). *ECS Transactions*, *107*(1), 5655.

XL. Kabat, S. R., Panigrahi, C. K., & Ganthia, B. P. (2022). Comparative analysis of fuzzy logic and synchronous reference frame controlled LVRT capability enhancement in wind energy system using DVR and STATCOM. In *Sustainable Energy and Technological Advancements: Proceedings of ISSETA 2021* (pp. 423-433). Singapore: Springer Singapore.

XLI. Kabat, S. R., Panigrahi, C. K., Ganthia, B. P., Barik, S. K., & Nayak, B. (2022). Implementation and analysis of mathematical modeled drive train system in type III wind turbines using computational fluid dynamics. *Advances in Science and Technology. Research Journal*, *16*(1), 180-189.

XLII. Kabat, Subash Ranjan, and Bibhu Prasad Ganthia, Chinmoy Kumar Panigrahi. "Fuzzy Logic and Synchronous Reference Frame Controlled LVRT Capability Enhancement in Wind Energy System using DVR." *Turkish Journal of Computer and Mathematics Education (TURCOMAT)* 12.6 (2021): 4899-4907.

XLIII. Khan, M. A., Prasad, R., and Zhang, L., "A Transformerless Multilevel Inverter Using Switched-Capacitor Units for Grid Integration," *IEEE Transactions on Power Electronics*, vol. 39, no. 2, pp. 1123–1135, Feb. 2024, 10.1109/TPEL.2023.3356210.

XLIV. Khounjahan, H., Abapour, M., and Zare, K., "Switched-capacitor based single source cascaded h-bridge multilevel inverter featuring boosting ability," *IEEE Trans. Power Electron.*, vol. 34, no. 2, pp. 1113–1124, Feb. 2019.

XLV. L Vadivel Kannan, J. N. D. D. V. M. M. S. R. K. Ganthia, B. P., N. C. R., . (2021). Cascade H Bridge Multilevel Inverter with Pwm for Lower Thd, Emi & Rfi Reduction. *Annals of the Romanian Society for Cell Biology*, *25*(6), 2972–2977. https://www.annalsofrscb.ro/index.php/journal/article/view/6013.

XLVI. Lee, S. S., Bak, Y., and Kim, S. M., "New Family of Boost Switched-Capacitor 7-Level Inverters (BSC7LI)," *IEEE Transactions on Power Electronics*, vol. 33, no. 11, pp. 10471–10479, 2019.

XLVII. Liu, J., Zhu, X., and Zeng, J., "A seven-level inverter with self-balancing and low-voltage stress," *IEEE J. Emerg. Sel. Topics Power Electron.*, vol. 8, no. 1, pp. 685–696, Mar. 2020, 10.1109/JESTPE.2018.2879890.

XLVIII. Maherchandani, J. K., Joshi, R. R., Tirole, R., Swami, R. K., & Ganthia, B. P. (2022). Performance Comparison Analysis of Energy Management Strategies for Hybrid Electric Vehicles. In *Recent Advances in Power Electronics and Drives: Select Proceedings of EPREC 2021* (pp. 245-254). Singapore: Springer Nature Singapore.

XLIX. Mannam P, Manchireddy S, Ganthia BP. Grid Tied PV with Reduced THD Using NN and PWM Techniques. Design Engineering. 2021 Jun 6:2019-27.

L. Mehta, S. B. and Rout, T. J., "Hybrid Control of a Self-Charging Switched-Capacitor Based Seven-Level Inverter for PV Systems," *IEEE Access*, vol. 12, pp. 21789–21798, 2024. 10.1109/ACCESS.2024.3357892.

LI. Mishra, S., Ganthia, B. P., Sridharan, A., Rajakumar, P., Padmapriya, D., & Kaliappan, S. (2022). Optimization of load forecasting in smartgrid using artificial neural network based NFTOOL and NNTOOL. In *Journal of Physics: Conference Series* (Vol. 2161, No. 1, p. 012068). IOP Publishing.

LII. Mohanty, M., Nayak, N., Ganthia, B. P., & Behera, M. K. (2023, June). Power Smoothening of Photovoltaic System using Dynamic PSO with ESC under Partial Shading Condition. In *2023 International Conference in Advances in Power, Signal, and Information Technology (APSIT)* (pp. 675-680). IEEE.

LIII. Narayan, V., Reddy, K. C., and Lee, H., "Optimized PWM for a Self-Balancing Seven-Level Switched-Capacitor Inverter in EV Charging Applications," *IEEE Transactions on Transportation Electrification*, vol. 10, no. 1, pp. 612–621, Mar. 2024. 10.1109/TTE.2023.3342084.

LIV. Pahadasingh, S., Jena, C., Panigrahi, C. K., & Ganthia, B. P. (2022). JAYA Algorithm-Optimized Load Frequency Control of a Four-Area Interconnected Power System Tuning Using PID Controller. *Engineering, Technology & Applied Science Research*, *12*(3), 8646-8651.

LV. Peng, W., Ni, Q., Qiu, X., and Ye, Y., "Seven-Level Inverter with Self-Balanced Switched-Capacitor and Its Cascaded Extension," *IEEE Transactions on Power Electronics*, vol. 34, no. 12, pp. 11889–11896, 2019.

LVI. Pragati, A., Ganthia, B.P., Panigrahi, B.P. (2021). Genetic Algorithm Optimized Direct Torque Control of Mathematically Modeled Induction Motor Drive Using PI and Sliding Mode Controller. In: Kumar, J., Jena, P. (eds) Recent Advances in Power Electronics and Drives. Lecture Notes in Electrical Engineering, vol 707. Springer, Singapore. 10.1007/978-981-15-8586-9_32.

LVII. Pritam, A., Sahu, S., Rout, S. D., Ganthia, S., & Ganthia, B. P. (2017, August). Automatic generation control study in two area reheat thermal power system. In *IOP Conference Series: Materials Science and Engineering* (Vol. 225, No. 1, p. 012223). IOP Publishing.

LVIII. Priyadarshini, L., Kundu, S., Maharana, M. K., & Ganthia, B. P. (2022). Controller Design for the Pitch Control of an Autonomous Underwater Vehicle. *Engineering, Technology & Applied Science Research*, *12*(4), 8967-8971.

LIX. Refaai, M. R. A., Dhanesh, L., Ganthia, B. P., Mohanty, M., Subbiah, R., & Anbese, E. M. (2022). Design and Implementation of a Floating PV Model to Analyse the Power Generation. *International Journal of Photoenergy*, *2022*.

LX. Rubavathy, S. J., Venkatasubramanian, R., Kumar, M. M., Ganthia, B. P., Kumar, J. S., Hemachandu, P., & Ramkumar, M. S. (2021, September). Smart Grid Based Multiagent System in Transmission Sector. In *2021 Third International Conference on Inventive Research in Computing Applications (ICIRCA)* (pp. 1-5). IEEE.

LXI. Sahu, P. K., Mohanty, A., Ganthia, B. P., & Panda, A. K. (2016, January). A multiphase interleaved boost converter for grid-connected PV system. In *2016 International Conference on Microelectronics, Computing and Communications (MicroCom)* (pp. 1-6). IEEE.

LXII. Sahu, S., Mohapatra, B. K., Kabat, S. R., Panda, S., Pahadasingh, S., & Ganthia, B. P. : "MULTIPLE ORDER HARMONIC ELIMINATION IN PHOTO VOLTAIC SYSTEM USING SPWM BASED ELEVEN LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER."

LXIII. Samal, S. K., Jena, S., Ganthia, B. P., Kaliappan, S., Sudhakar, M., & Kalyan, S. S. (2022). Sensorless Speed Contorl of Doubly-Fed Induction Machine Using Reactive Power Based MRAS. In *Journal of Physics: Conference Series* (Vol. 2161, No. 1, p. 012069). IOP Publishing.

LXIV. Satpathy, S.R., Pradhan, S., Pradhan, R., Sahu, R., Biswal, A.P., Ganthia, B.P. (2021). Direct Torque Control of Mathematically Modeled Induction Motor Drive Using PI-Type-I Fuzzy Logic Controller and Sliding Mode Controller. In: Udgata, S.K., Sethi, S., Srirama, S.N. (eds) Intelligent Systems. Lecture Notes in Networks and Systems, vol 185. Springer, Singapore. 10.1007/978-981-33-6081-5_21.

LXV. Siddique, M. D., Ali, J. S. M., Mekhilef, S., Mustafa, A., and Sandeep, N., "Reduce Switch Count Based Single Source 7L Boost Inverter," *IEEE Transactions on Circuits and Systems II: Express Briefs*. 10.1109/TCSII.2020.2988090.

LXVI. Sun, X., Wang, B., Zhou, Y., Wang, W., Du, H., and Lu, Z., "A single dc source cascaded seven-level inverter integrating switched-capacitor techniques," *IEEE Trans. Ind. Electron.*, vol. 63, no. 11, pp. 7184–7194, Nov. 2016.

LXVII. Taghvaie, A., et al., "A Self-balanced step-up multilevel inverter based on switched-capacitor structure," *IEEE Trans. Power Electron.*, vol. 33, no. 1, pp. 199–209, Jan. 2018.

LXVIII. Thenmalar, K., K. Kiruba, Praveen Raj, and Bibhu Prasad Ganthia. "A Real Time Implementation of ANN Controller to Track Maximum Power Point in Solar Photovoltaic System." *Annals of the Romanian Society for Cell Biology* 25, no. 6 (2021): 10592-10607.

LXIX. Xie, Hui, Yatao Wang, Zhiliang Gao, Bibhu Prasad Ganthia, and Chinh V. Truong. "Research on frequency parameter detection of frequency shifted track circuit based on nonlinear algorithm." *Nonlinear Engineering* 10, no. 1 (2021): 592-599.

LXX. Zheng, W., Mehbodniya, A., Neware, R., Wawale, S. G., Ganthia, B. P., & Shabaz, M. (2022). Modular unmanned aerial vehicle platform design: Multi-objective evolutionary system method. *Computers and Electrical Engineering*, *99*, 107838.