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ALL-OPTICAL CARRY SKIP ADDER WITH THE HELP OF TERAHERTZ OPTICAL ASYMMETRIC DEMULTIPLEXER-BASED SWITCH

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Abstract

The terahertz optical asymmetric demultiplexer (TOAD) or semiconductor optical amplifier (SOA)-assisted Sagnac switches have been used to construct an all-optical 4-bit carry skip adder. This design aims to satisfy the high speed and accuracy requirements of modern ultrafast digital transmission. Using a combination of an all-optical multiplexer and an all-optical full adder, we describe an all-optical carry skip adder. When compared to ripple carry adder and carry look-ahead adder, carry skip adder may be employed to create a fast arithmetical processing unit. Numerical simulation is used to develop and validate this theoretical model.

Keywords: Terahertz optical asymmetric demultiplexer; semiconductor optical amplifier; carry skip adder; optical logic.

I. Introduction

In all-optical logic and signal processing, semiconductor optical amplifiers (SOAs) are among the most significant research topics [II-V]. They can carry out a wide range of operations, including regeneration, time-division demultiplexing, and Boolean logic and arithmetic operations [VI–XIII], thanks to their compactness, simplicity, massive nonlinearities, and ease of integration. The dynamics of optically generated carriers control the nonlinearities that make SOAs useful in these applications. The most popular arithmetic operation is addition, and adders carry out some of the most important tasks for any digital processor, hence rigorous optimization is required to increase the performance of this operation. The transistor sizes and circuit architecture are already being adjusted to achieve this optimization at the gate or circuit level consider altering the Boolean equations to produce a quicker or smaller circuit with even lower power consumption. To achieve the ideal area, latency, and power requirements, several adder topologies including ripple carry adder, carry-lookahead adder, carry choose adder, conditional sum, and other parallel prefix adders are being produced. The simplest adder, ripple carry, has the largest time delay, O(n), where n is the bit size of the operands. The area and delay for our circuit are both O (n log n). When it comes to delay, our circuit design performs

better. In this article, an all-optical 4-bit carry skip adder is designed using a switch based on a terahertz optical asymmetric demultiplexer (TOAD).

II. Operation of TOAD-Based Switch

The basic structure of TOAD based switch is shown in Fig. 1 [XIV, XV].

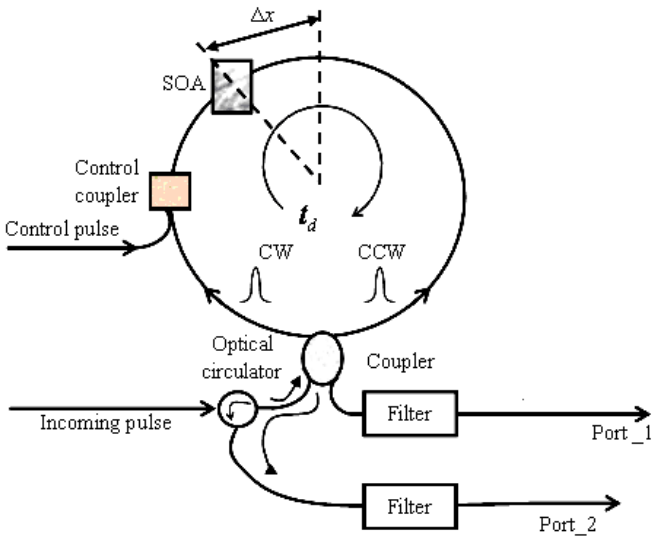

Fig.1. A TOAD-based optical switch with a single control pulse (CP), where SOA: Semiconductor optical amplifier, CW: Clockwise pulse, CCW: Counterclockwise pulse, and Δx: is asymmetric distance

this paper, we have tried to use the output from both the transmitting and reflecting mode of the device. The output power at port_1 and port_2 can be expressed as [XVI-XVIII]

$$P_{out\_1}(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) - 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \quad (1)$$

$$P_{out\_2}(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) + 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \quad (2)$$

where, $G_{cw}(t), G_{ccw}(t)$ is the power gain. The time-dependent phase difference between clockwise (CW) and counter-clockwise (CCW) pulses [XVI] is

$$\Delta\varphi = -\alpha/2 \cdot \ln\left(G_{cw}(t)/G_{ccw}(t)\right) \quad (3)$$

with α being the line-width enhancement factor. In the absence of a control signal, data signal (incoming signal) enters the fiber loop, passes through the SOA at

different times as they counter-propagate around the loop, and experience the same unsaturated small amplifier gain G_{ss}, and recombine at the input coupler i.e. $G_{ccw} = G_{cw}$. Then, $\Delta\varphi = 0$ and expression for $P_{out\_1}(t) = 0$ and $P_{out\_2}(t) = P_{in}(t) \cdot G_{ss}$. It shows that data is reflected toward the source. When a control pulse is injected into the loop, it saturates the SOA and changes its index of refraction. The gain of SOA decreases rapidly [XV-XVII]. As a result, the two counter-propagation data signals will experience differential gain saturation profiles i.e. $G_{ccw} \neq G_{cw}$. Therefore they recombine at the input coupler, and then $\Delta\varphi \approx -\pi$ the data will exit from the output port-1 i.e. $P_{out\_1}(t) \neq 0$, and $P_{out\_2}(t) \approx 0$, the corresponding values can be obtained from the equation (2). The energy of the control pulse is ten times greater than that of the incoming pulse. A filter may be used at the output TOAD-based switch to reject the control and pass the incoming pulse.

III. All Optical Full Adder

A full adder adds binary integers while taking into consideration both carried-in and carried-out values. Three one-bit values, commonly represented as A, B, and Cin, are added by a one-bit full-adder (FA). The operands are A and B, and Cin is a one-bit brought in (theoretically from a previous edition). A two-bit output sum is generated by the circuit, and it is commonly represented by the signals Cout (carry) and S (sum). The full-adder's block diagram and all-optical circuit are seen in Figs. 2 and 3, respectively. Gayen and Roy [II] suggest a detailed operation.

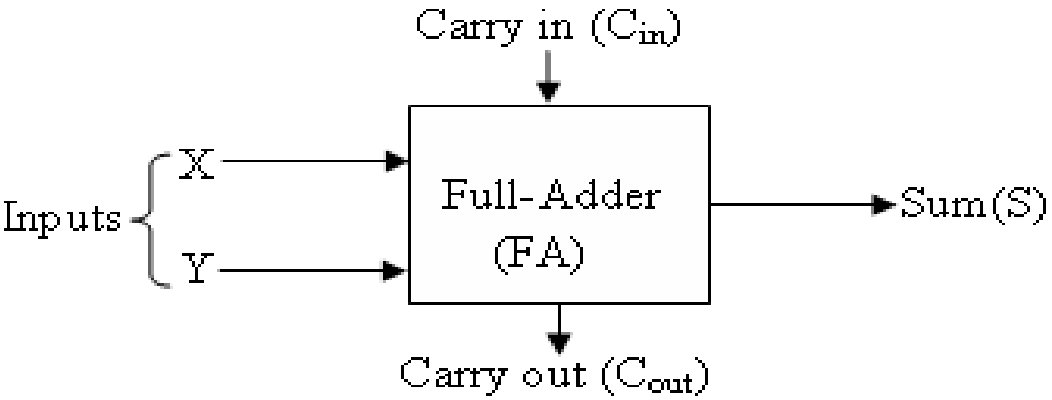

Fig.2. Block diagram of the full adder (FA).

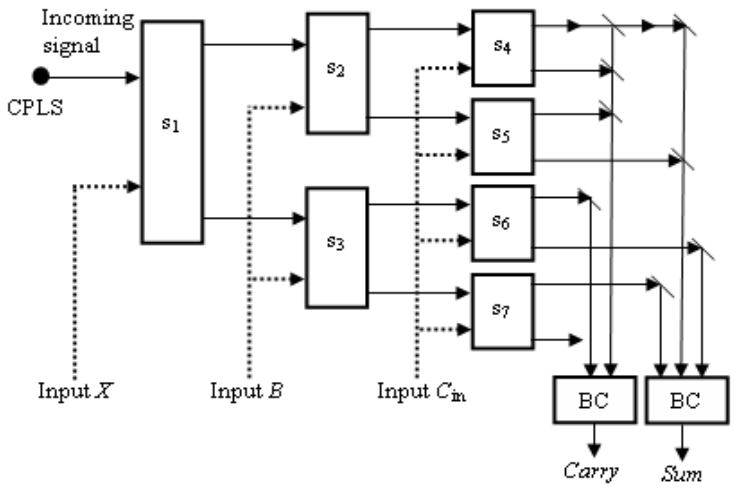

Fig.3. All-optical integrated full-adder [18], where CPLS: Constant pulse light source, *A*, *B*, and C_{in}: Input signals, s_1-s_7: TOAD based switches, BC: Beam combiner, \ : beam splitter, *Carry* and *Sum*: Final outputs

The outputs are derived from Sum and Carry depending on the state of the input variables (A, B, Cin) [these are also the light signals]. These outputs' logical expression is as follows:

$$\begin{aligned} S &= ABC_{in} + A\bar{B}\bar{C}_{in} + \bar{A}B\bar{C}_{in} + \bar{A}\bar{B}C_{in} \\ &= \left(A \oplus B \oplus C_{in}\right) \end{aligned} \tag{4}$$

$$\begin{aligned} C_{out} &= ABC_{in} + AB\overline{C_{in}} + A\bar{B}C_{in} + \bar{A}BC_{in} \\ &= C\left(A \oplus B\right) + AB \end{aligned} \tag{5}$$

IV. All Optical Multiplexer

A multiplexer (MUX) is a combinational circuit that is given a specified number of data inputs (often a maximum power of 2) and n address inputs (select inputs), which are used as a binary number to pick one of the data inputs. Let's suppose that the number of data inputs is 2n. A single output from the MUX has the same value as the chosen data input. The 2×1 MUX's all-optical operating concept is described in Fig. 4. We employ TOAD-based optical switches, namely s_1 through s_3, which have one select input (S_0) and two data inputs (D_0 and D_1), to build optical 2×1 MUX. Fig. 5 depicts the block diagram of a 2×1 multiplexer.

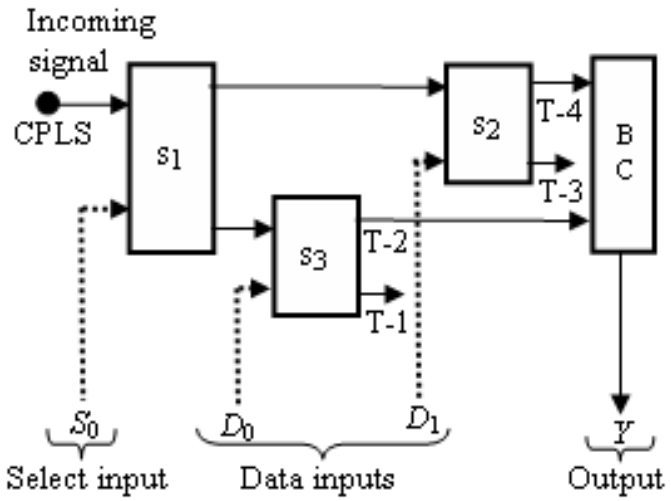

Fig.4. A unit-wise block diagram of all-optical 2×1 multiplexer, where CPLS: Constant pulse light source, S_0: Select input, D_0, and D_1: Data inputs, s_1-s_3: TOAD-based switches, T-1 through T-4: Output terminals, BC: Beam combiner, and *Y*: Final output.

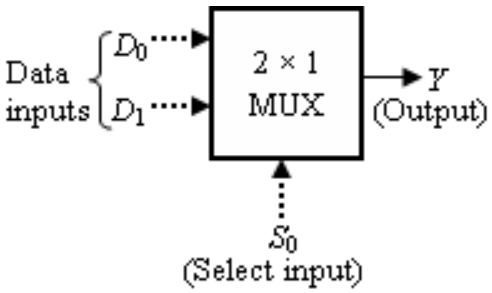

Fig.5. The block diagram of 2×1 multiplexer (MUX)

We can direct the input data signal to one of the necessary output channels by applying the right control signal. Here, the control signal S_0 serves as a select input, D_0 and D_1 are the input data signals, and Y is the output signal in the multiplexing scheme. A certain input data signal (D_0 or D_1) is chosen based on the appropriate value of the control signal S_0, and this input data signal is then transmitted to the output Y. These next two scenarios are possible. Switch S_1 receives light from the Constant Pulse Light Source (CPLS) when $S_0 = 0$. Since S_0 is not receiving a control signal, the light enters S_1's lower channel and falls on S3's switch. and the light does not enter any other channel. The input data for switch s_3 is D_0. Now, if $D_0 = 0$, T-1 will be in the 1-state, while T-2, T-3, and T-4 will be in the 0-state.

With the aid of a beam combiner BC, the terminals T-2 and T-4 are combined to create the final output. As a result, the output is dark, or Y = 0. The light beam reaches the beam combiner BC if $D_0 = 1$, at which point T-2 is in the 1-state and the remaining terminals (T-1, T-3, and T-4) are in the 0-state. At the output, the light is present, so Y = 1. As a result, we deduce that $Y = D_0$ when $S_0 = 0$. Consequently, the input data D_0 can Set $S_0 = 0$ to send data to output Y.

The light from CPLS, on the other hand, incidence on switch s1 first when $S_0 = 1$. The light enters the top channel of s_1 and falls on s_2 when $S_0 = 1$. The input data for switch s_2 is D_1. Now, if $D_1 = 0$, T-3 will be in the 1-state, while T-1, T-2, and T-4 will be in the 0-state. There is therefore no light at output Y.

The light beam reaches the beam combiner BC if $D_1 = 1$, at which point T-4 is in the 1-state and the remaining terminals (T-1, T-2, and T-3) are in the 0-state. As a result, Y = 1 indicates that there is light at the output. So, we get the conclusion that $S_0 = 1$ and $Y = D_1$. This indicates that by setting $S_0 = 1$, the input data D_1 may be transmitted to the output Y. This is how a multiplexer is created using all-optical switches based on TOAD. The output of a multiplexer is logically expressed as

$$Y = S_0 D_1 + \bar{S}_0 D_0 \tag{6}$$

V. Design of All-Optical Carry Skip

The use of a ripple-carry adder for long word lengths is completely impractical because it is linearly dependent on the carry of each block addition, which means they carry bit is "rippled" from one stage to the next. As a result, the delay through the circuit depends on the number of logic stages that must be crossed and is a function of the applied input signals. To get around this, we created an adder that concurrently calculates the addition of the next two bits, cutting down on gate delays. By skipping over clusters of adjacent adder stages, a carry-skip adder shortens the carry-propagation time. This adder concurrently adds over the following two bits while taking into account two carry options, 1 or 0, and adding the current bit by the least substantial bit (LSB). This approach adds the following two bits without taking into account the carry from the LSB, making it quicker than a ripple carry adder. Using full adders (FA) and 2X1 multiplexers (MUX), a 4-bit carry skip adder is demonstrated in Fig. 6.

In this circuit, the first two LSB (A_0, A_1, B_0, and B_1) of each number are added using a pair of two full adders (FA-1 and FA-2), and the next two bits are added concurrently using two sets of two full adders, respectively, while taking into account the values of $c_0 = 1$ and $c_0 = 0$. Using two full adders and the carry cin, bits A_0 and A_1 are added to bits B_0 and B_1 in this circuit, respectively. The full adder FA-1 creates the output S_0 and carries for the full adder FA-2 from the three inputs A_0, B_0, and Cin. Once more, full adder FA-2 accepts the three inputs from FA-1 as A_1, B_1, and carryout and produces S_1 and carryout as its output. The select lines for the

multiplexers MUX-1, MUX-2, and MUX-3 are served by this carryout. In parallel with this operation, full adder FA-3 accepts the three inputs A_2, B_2, and $C_0 = 1$ and generates an output that serves as a data line D1 for MUX-1 and a carry for full adder FA-4. Similar to this, the multiplexer MUX-2 and MUX-3 use the output and carry from FA-4 as their respective data lines D_1 and D_2, respectively. Like this, the output from FA-5, the output and carry from FA-6, and the multiplexers MUX-1, MUX-2, and MUX-3 each function as a data line D0. The outputs S_2, S_3, and Cout are produced by MUX-1, MUX-2, and MUX-3, respectively, depending on the value of the select line s. Therefore, Cout$S_3S_2S_1S_0$ is the circuit's final output.

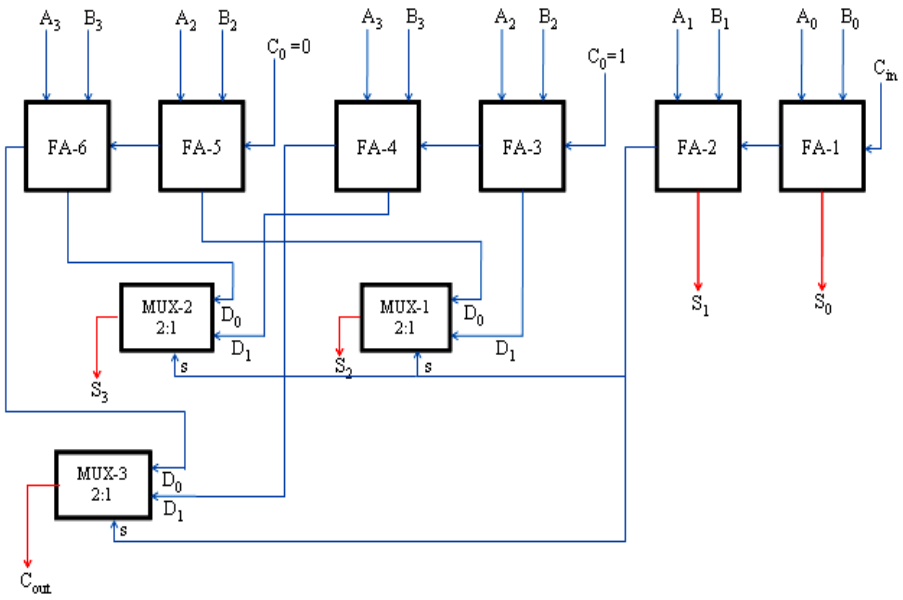

Fig. 6. Block diagram of all-optical carry skip adder.FA: full adder, MUX: 2×1 multiplexer.

Consider the following scenario: A is 1100 ($A_3A_2A_1A_0$), B is 1001 ($B_3B_2B_1B_0$), and C_{in} is 0. $S_0 = 1$ and $S_1 = 0$, following the complete adder's operating principle. If the select input for the three multiplexers has the value 0, or s = 0, then. Therefore, the data line D_0 will be chosen for all multiplexers. In this instance, the multiplexes MXU-1, MUX-2, and MUX-3's outputs S_2, S_3, and Cout each get the values 1, 0, and 1, respectively. The result is therefore 10101 (Cout$S_3S_2S_1S_0$). Similar to this, the carry skip adder is used to add any two 4-bit values.

VI. Simulated Results

The simulation's input parameters are as follows: the SOA's unsaturated amplifier gain (Gss) = 30 dB, the SOA's gain recovery time (τ_e) = 90 ps, the SOA's saturation energy (Esat) = 700 fJ, the eccentricity of the loop (Tasym) = 30 ps, the line-width enhancement factor (α)= 6, the full width at half maximum of the control

pulse (σ)= 6 ps, the bit period (Tc) = 100 ps, and the control pulse energy (Ecp) = 70 fJ, which must satisfy the operational conditions. Fig. 7 displays the simulated input and output waveforms.

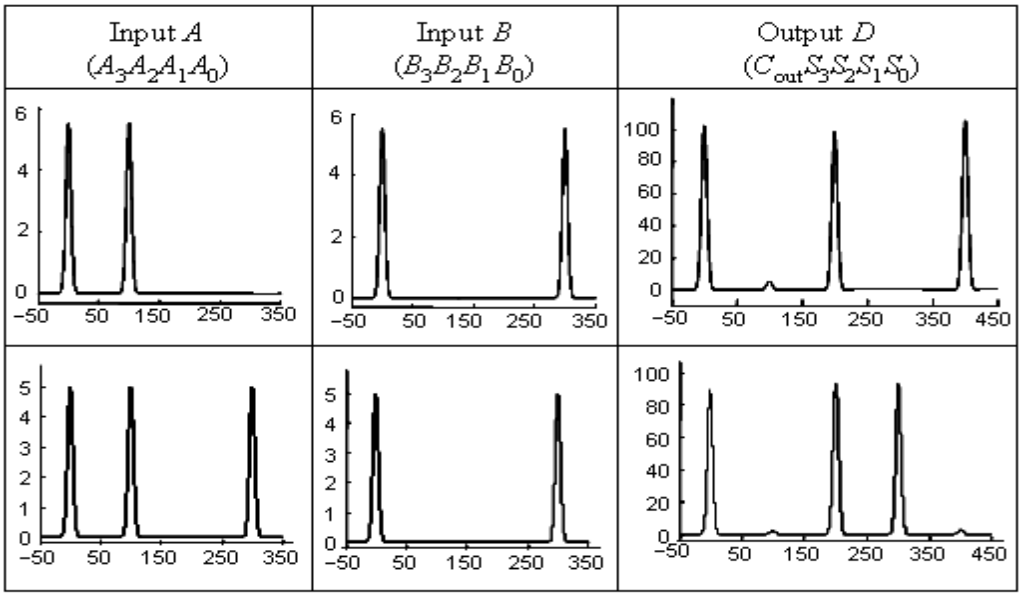

Fig. 7. Simulated input and output waveforms, power (mW) is along the y-axis and time is along the x-axis in ps.

VII. Conclusion

In this work, we present a brand-new TOAD-based carry skip adder design. The key benefit of this suggested approach is that the converter circuit may carry out addition operations, which are entirely optical in nature. In comparison to ripple carry adders and carry look-ahead adders, a fast-processing unit may be created using this carry skip adder design. Through numerical simulation, this theoretical model has been validated.

Conflict of Interest:

There was no conflict of interest regarding this paper

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