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ALL-OPTICAL PARALLEL HALF ADDER USING TERAHERTZ OPTICAL ASYMMETRIC DEMULTIPLEXER

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Abstract

Using TOAD based switch we have designed a parallel half-adder. The approach to designing all-optical arithmetic circuits not only enhances the computational speed but is also capable of synthesizing light as input to produce the desired output. The main advantage of a parallel circuit is the synchronization of input is not required. All the circuits are designed theoretically and verified through numerical simulations.

Keywords: Terahertz optical asymmetric demultiplexer; semiconductor optical amplifier; half adder; optical logic.

I. Introduction

Now a day high-speed all-optical logic gates are crucial devices in optical networks because they execute essential signal processing functions such as switching regeneration and header recognition processing in photonic switching nodes. A revolution has been brought about in all-optical information processing systems with the help of the discovery of ultra-high-speed all-optical switches based on cross-phase modulation (XPM) [I-IV]. Among different optical switches, the terahertz optical asymmetric demultiplexer (TOAD)/semiconductor optical amplifier (SOA)-assisted Sagnac gate effectively combines fast switching time, high repetition rate, and low power consumption [V-X]. In this paper, we propose and describe the all-optical parallel half adder using TOAD-based all-optical switches. We have utilized both the transmitted and reflected ports of the device.

II. Operation of TOAD-based switch

The basic design of TOAD based switch is shown in Fig. 1 [XI, XII]. Here a nonlinear element (NLE) is placed asymmetrically in a loop. The coon NLE is a semiconductor optical amplifier (SOA). In this paper, we have tried to use the output from both the transmitting and reflecting modes of the device. The output power at the upper and lower can be expressed as [XIII-XV]

$$P_{Upper}(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) - 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \quad (1)$$

$$P_{Lower}(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) + 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \quad (2)$$

where, $G_{cw}(t), G_{ccw}(t)$ is the power gain. The time-dependent phase difference between clockwise (CW) and counterclockwise (CCW) pulses [XIII] is $\Delta\varphi = -\alpha/2 . \ln(G_{cw}(t)/G_{ccw}(t))$ with α being the line-width enhancement factor.

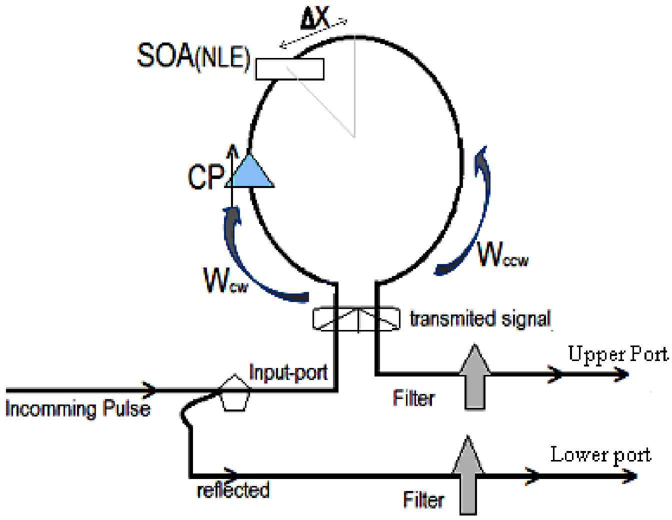

Fig. 1. A TOAD-based optical switch with single control pulse (CP), where SOA: Semiconductor optical amplifier, CW: Clockwise pulse, CCW: Counterclockwise pulse, and Δx: asymmetric distance.

In the absence of a control signal, data signal (incoming signal) enters the fiber loop, passes through the SOA at different times as they counter-propagate around the loop, experience the same unsaturated small amplifier gain G_{ss} , and recombine at the input coupler i.e. $G_{ccw} \approx G_{cw}$. Then, $\Delta\varphi \approx 0$ and expression for $P_{Upper}(t) \approx 0$ and $P_{Lower}(t) = P_{in}(t) \cdot G_{ss}$. It shows that data is reflected back toward the source. When a control pulse is injected into the loop, it saturates the SOA and changes its index of refraction. The gain of SOA decreases rapidly [XIII-XV]. As a result, the two counter-propagation data signals will experience differential gain saturation profiles i.e. $G_{ccw} \neq G_{cw}$. Therefore they recombine at the input coupler, and then $\Delta\varphi \approx -\pi$ the data will exit from the upper port i.e. $P_{Upper}(t) \neq 0$, and $P_{Lower}(t) \approx 0$, the corresponding values can be obtained from the equation (2). The energy of the control pulse is ten times greater than that of the incoming pulse. A filter may be used at the output of TOAD based switch to reject the control and pass the incoming pulse. The schematic diagram of TOAD based switch is shown in Fig. 2.

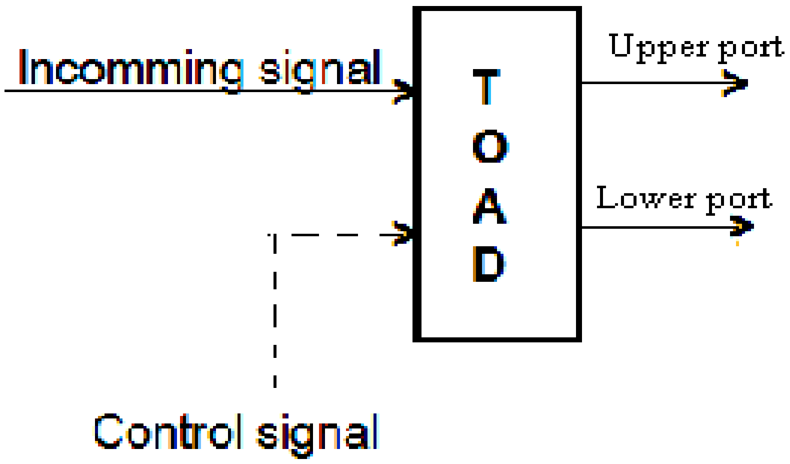

Fig. 2. The schematic diagram of TOAD based switch

III. All-Optical Parallel Half Adder

A half-adder circuit adds two one-bit binary numbers (A and B) and gives the output of two one-bit binary numbers, a sum (S) and a carry (Cout). The operational principle of the all-optical parallel half adder is shown in Fig. 3. To implement this circuit, we use TOAD-based switches namely, T1 to T4.

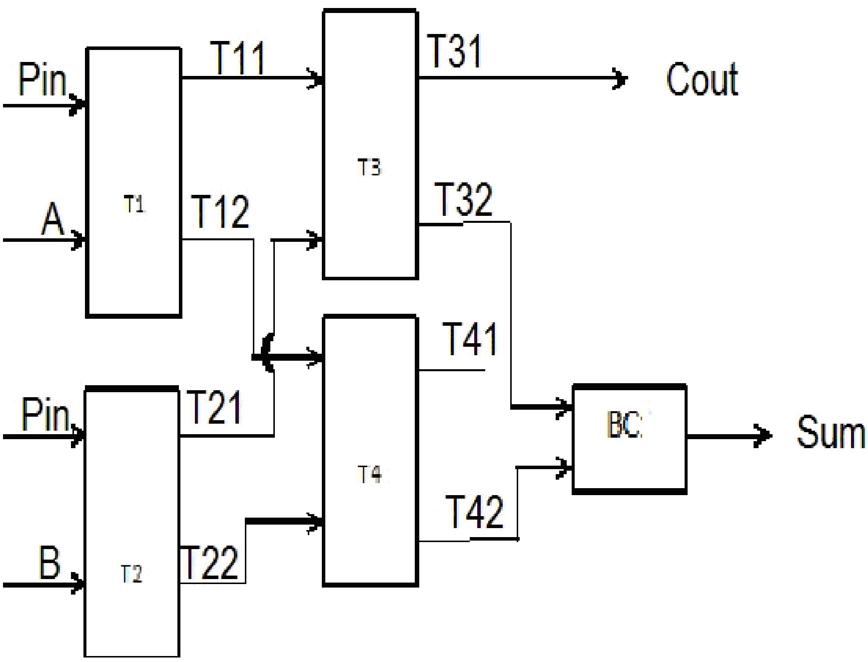

Fig. 3. All-optical parallel half adder

There are 4 different input combinations for implementing double-input binary logic. Depending on the state of input variables (A and B) [These are the light signals]. The output of the corresponding circuit is obtained from Beam Combiner (BC) as Sum and T31 as Cout. Four Cases are described below in detail.

CASE 1: When A = 0 and B = 0. Light from the Pin is incident on switches T1 and T2. As the control signals A, and B is absent light emerges through the lower channel of T1, and T2 as T12 = 1, and T22 = 1 respectively. T21 = 0 and T22 = 1 falls on lower channel of T3 and T4 respectively and T11 = 0 and T12=1 falls on upper channel of T3 and T4 respectively, produces output as T31 = 0, T32 = 0, T42 = 0. Now T32 and T42 feed to BC to get output as Sum = 0. Upper output channel of switch T3 i.e., T31 produces Cout = 0.

CASE 2: When A = 0 and B = 1. Light emerges out from T42 only i.e., from the lower output channel of switch T4. So, T31 and T32 become 0. Hence Sum = 1 (T42 + T32) and Cout = 0 (T31).

CASE 3: When A = 1 and B = 0. Light emerges out from T32 only i.e., from the lower output channel of switch T3. So, T31 and T42 become 0. Hence Sum = 1 (T42 + T32) and Cout = 0 (T31).

CASE 4: When A = 1 and B = 1. Light emerges out from T31 only i.e., from the upper output channel of switch T3. So, T32 and T42 become 0. Hence Sum = 0 (T42 + T32) and Cout = 1 (T31).

Hence, Sum = $(A \oplus B)$ and Cout = AB. In this way, the addition of any two-bit number can be done with this circuit.

IV. Results and Discussion

The parameters used in this simulation are taken from the literature survey of different research papers [X, XIII-XV]. The values of different parameters as unsaturated amplifier gain of the SOA (Gss) = 30 dB, gain recovery time of SOA (τ_e) = 90 ps, saturation energy of the SOA (Esat) = 700 fJ, the eccentricity of the loop (T_{asym}) = 30 ps, line-width enhancement factor (α) = 6, full width at half maximum of control pulse (σ) = 6 ps, bit period (T_c) = 100 ps, and a control pulse energy (E_{cp}) = 70 fJ so that the operational conditions are satisfied. The simulated input and output waveforms of the half-adder are shown in Fig. 5.

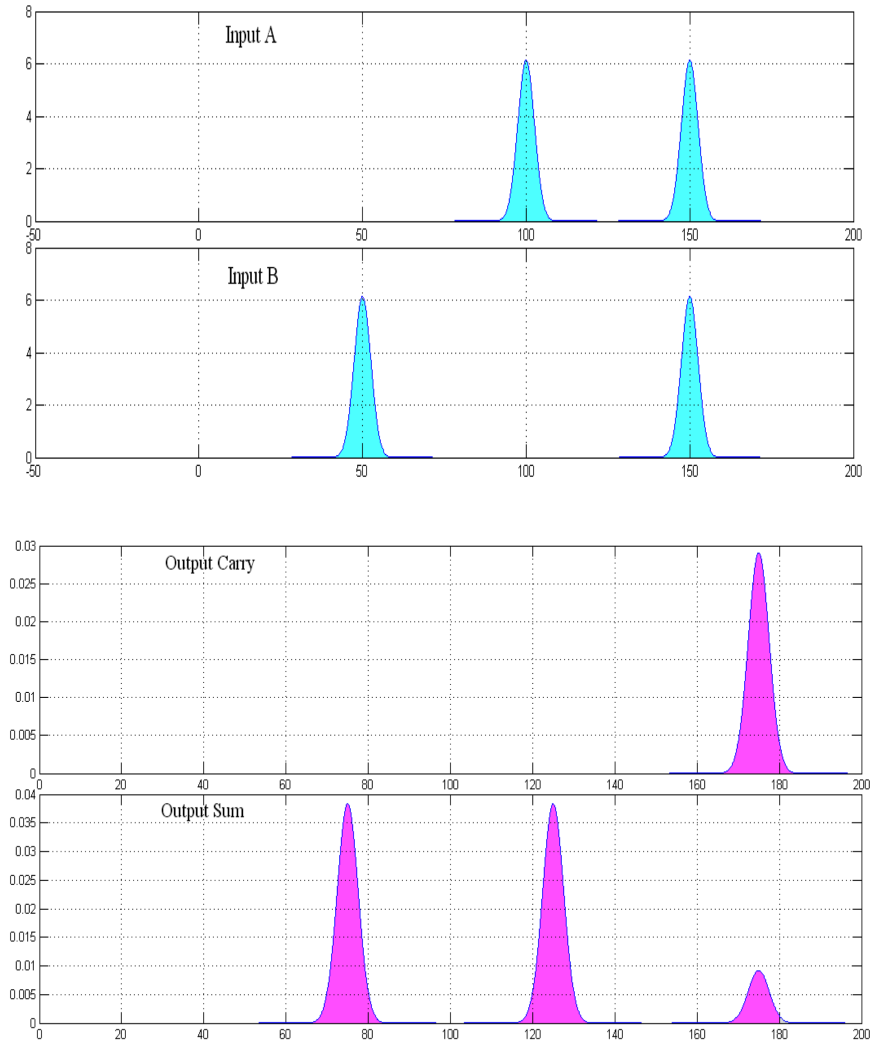

Fig. 5. Simulated input and output waveforms of a parallel half adder, where power is along the y-axis whereas time is along the x-axis.

V. Conclusions

In this paper, we have reported a novel design of a parallel all-optical half-adder. Here, in this proposed scheme, the significant advantage is that the proposed circuit can perform additional operations, which are all-optical in nature. This theoretical model has been verified through numerical simulation.

Conflicts of Interest:

There is no conflict of interest regarding this article.

Reference

I. A. Bhattacharyya, D. K. Gayen, and T. Chattopadhyay, “4-bit All-optical Binary to Two’s Complement Converter”, *Proceedings of International Conference on Communications, Devices and Intelligent Systems, 496 - 499 (2012)*. 10.1109/CODIS.2012.6422247

II. A. Bhattacharyya, D. K. Gayen, and T. Chattopadhyay, “Alternative All-optical Circuit of Binary to BCD Converter Using Terahertz Asymmetric Demultiplexer Based Interferometric Switch”, *Proceedings of 1st International Conference on Computation and Communication Advancement (IC3A-2013)*.

III. A. Bhattacharyya, D. K. Gayen, ALL-OPTICAL N-BIT BINARY TO TWO’S COMPLEMENT CONVERTER WITH THE HELP OF SEMICONDUCTOR OPTICAL AMPLIFIER-ASSISTED SAGNAC SWITCH. *J. Mech. Cont. & Math. Sci., Vol.-17, No.-1, January (2022) pp 117-125*. 10.26782/jmcms.2022.01.00009.

IV. A. M. Melo, J. L. S. Lima, R. S. de Oliveira, and A. S. B. Sombra, “Photonic time Division Multiplexing (OTDM) using Ultra-short Picosecond Pulses in a Terahertz Optical Asymmetric Demultiplexer (TOAD)”, *Optics Communications, 205(4-6), 299-312 (2002)*. 10.1109/SBMOMO.2001.1008820

V. B. Wang, V. Baby, W. Tong, L. Xu, M. Friedman, R. Runser, I. Glesk, and P. Prucnal, “A novel fast optical switch based on two cascaded terahertz optical asymmetric demultiplexers (TOAD)”, *Optics Express, 10(1), 15-23 (2002)*.

VI. D. Cotter, R.J. Manning, K.J. Blow, A.D. Ellis, A.E. Kelly, D. Nesset, I. D. Phillips, A. J. Poustie, D.C. Rogers, “Nonlinear optics for high-speed digital information processing,” *Science 286, 1523-1528 (1999)*.

VII. D. K. Gayen, T. Chattopadhyay, M. K. Das, J. N. Roy, and R. K. Pal, “All-optical binary to gray code and gray to binary code conversion scheme with the help of semiconductor optical amplifier -assisted sagnac switch”, *IET Circuits, Devices & Systems, 5(2), 123-131 (2011)*.

VIII. G. Li, “Recent advances in coherent optical communication”, *Advances in Optics and Photonics, 1(2), 279-307 (2009)*.

IX. H. L. Minh, Z. Ghassemlooy, and W. P. Ng, “Characterization and performance analysis of a TOAD switch employing a dual control pulse scheme in high speed OTDM demultiplexer”, *IEEE Communications Letters, 12(4), 316-318 (2008)*.

X. J. P. Sokoloff, P. R. Prucnal, I. Glesk, and M. Kane, "A terahertz optical asymmetric demultiplexer (TOAD)", IEEE Photonics Technology Letters, 5(7), 787-790 (1993).

XI. J. P. Sokoloff, P. R. Prucnal, I. Glesk, and M. Kane, "A terahertz optical asymmetric demultiplexer (TOAD)", IEEE Photonic Technology Letters, 5(7), 787-789 (1993).

XII. J. P. Sokoloff, I. Glesk, P. R. Prucnal, and R. K. Boneck, "Performance of a 50 Gbit/s optical time domain multiplexed system using a terahertz optical asymmetric demultiplexer", IEEE Photonics Technology Letters, 6(1), 98-100 (1994).

XIII. K. E. Zoiros, J. Vardakas, T. Houbavlis, and M. Moyssidis, "Investigation of SOA-assisted Sagnac recirculating shift register switching characteristics", *International Journal for Light and Electron Optics, 116(11), 527-541 (2005)*. 10.1016/j.ijleo.2005.03.005

XIV. M. Eiselt, W. Pieper, and H. G. Weber, "SLALOM: Semiconductor laser amplifier in a loop mirror", *Journal of Lightwave Technology, 13(10), 2099-2112 (1995)*. 10.1109/50.469721

XV. M Suzuki, H. Uenohara, "Invesigation of all-optical error detection circuitusing SOA-MZI based XOR gates at 10 Gbit/s", Electron. Lett. 45 (4), (2009).