

Effect of TCO, BSF and Back contact Barrier on CdS/CdTe solar cell: Modeling and Simulation

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Abstract

We have commenced an in-depth study through modeling and simulation to investigate the performance of a CdTe solar cell at different Schottky barrier heights for different combinations thicknesses of BSF as well as window layer and front contact oxide layer (TCO). The inter relation between BSF layer and back contact schottky barrier height has been focused. Effect of the BSF layer regarding the tunneling of charges has been investigated. In the present paper, we achieved in our study the highest η of 18.39%, V_{oc} of 0.591 volt, I_{sc} of 0.411 amp for 0.1 μm absorber and 1nm BSF layer thickness in presence of higher schottky barrier (0.6eV) with higher doping concentration of absorber layer. Thinning of the layers have always been better in terms of performance and cost. But it brings pinhole formation problems what we excluded here in our present work.

Keywords : Thin film solar, CdS/CdTe, TCO, Window layer, Schottky Barrier, Back Surface Field (BSF).

I. Introduction

In photovoltaic applications, CdTe solar cells have shown us, a new aspirant widow for large scale production. Antec GubH was concocted CdTe thin cell using CSS technology with CdS window layer. CdTe/CdS technologies have pretended the market a huge success over other photovoltaic materials. The trivial production cost of CdTe cells has patrolled it in the photovoltaic market. Though the efficiency of CdTe cells in the laboratory had shown only 16.5%, nevertheless it is seen with healthier efficiency in the contemporary research [IV, VIII, XIX, XXIV]. So CdTe gives us to develop the cost effective, stable and stanch thin film production for terrestrial applications. The focal aim of CdTe cell is to be settled with lesser material usage, transparent window layer and a compatible back contact layer which can provide good collections of the carriers at the terminals. It has been perceived that, CdS-CdTe cell is flexible, light weight and stable for elongated time with better performance. For this motivation, CdS-CdTe solar cell has been pledged for space applications these days [V].

CdS is one of the best translucent window layer and n-type hetero-structure material to p-CdTe. The wide band gap of CdS (2.4eV) tolerates broad spectrum of light into the cell conferring high efficiency. We can use very thin CdS layer to reduce the chances

of absorption and surface recombination. Excellent electrical comportment with high fill factor has been feasible by CdS-CdTe cell despite 10% lattice mismatch between CdS and CdTe. Its optoelectronic and chemical properties prepared it the best partner for p-CdTe. Fluorine doped Tin oxide ($\text{SnO}_2\text{:F}$) has been considered as the Transparent conducting oxide (TCO) and employed on top of the n-CdS layer considering high temperature deposition for low resistive front contact. It is transparent for large spectrum of light being a high band gap material [IV, VIII, XII-XIII]. We investigated on the CdS and TCO layer thicknesses to enhance the performance of the cell.

Truncated cost fabrication is a prime target today. Since CdTe has a high absorption coefficient ($>5 \times 10^5$) and direct optical band gap (1.45 eV), that is close to optimum band gap (1.5 eV) of solar cell, a very thin CdTe layer can harvest significant conversion efficiency with less carrier recombination being cost functioning for the fabrication and terrestrial usage too. As CdTe being a toxic material, thickness reduction ensures to be environmental friendly. Thinning lowers the production cost, time to produce the cell. It makes the productions cheaper and within your means. So, reduction of absorber and window layers has been one of the notable aims of the work considering the practical limitations. The CdTe thin film solar cells have been established experimentally for long-term resolute performance and high efficiency under AM1.5 illumination for terrestrial usage [IV, VI, VIII, X-XI, XIII-XIV, XX].

The main market mandate is to design low resistive back contact for P-CdTe. The electron affinity and band gap of P type CdTe together is quite high (≈ 5.7 eV). So an ohmic contact with any metal back contact has been almost unmanageable as P-CdTe always creates a sweeping schottky barrier with any metal contact. But contact barrier height does not depend only on work functions or electron affinity; rather there are influences of properties of the CdTe/metal interface region (defect states and Fermi level pinning). The schottky barrier affects (poor open circuit voltage and Fill Factor) the cell performance saturating the forward region current [III, VI-VIII, XX, XIV]. An eccentric process has been found to let perform a highly doped very thin CdTe layer as a BSF between p-CdTe and contact metal. The investigation on the highly doped p-CdTe layer has revealed the confinement and assortment of minority carrier having worked as an electron reflector either providing a relatively narrow schottky barrier or reducing barrier height that would succor to tunnel some extra holes resulting higher conversion efficiency (η), open circuit voltage (V_{oc}) and fill factor (FF) [I-II, IX, XIV-XV, XVII]. A unique investigation has been carried out for different rear contact barrier height along with varying BSF thickness that would help our continuing research to select proper contact metals or other contact materials for appropriate CdTe thickness in near future. Here, we did not comment on any particular metal rather we investigated on the effect of the barrier height at rear contact interface. Several factors like pinhole, leakage current and deposition processes are concerned with these parameters. Our investigation thus focused a light on it. But these are excluded for the work.

For deposition of CdS-CdTe cell, some of the well-used deposition techniques are close-space sublimation (CSS), chemical bath deposition (CBD), chemical vapor deposition (CVD). In addition chemical treatment and annealing rise the crystallibility of the device. For some specific cases, CdTe surface has been etched in such a manner that a Te-riched highly doped CdTe layer is formed at the CdTe/metal

interface. The etching processes have been effective for cleaning the surface along with smoothing and polishing. In addition these ensure us better stability of the cell making the layer good conducting with wider grain boundaries. The p+ region can be instigated to be deposited by etching (C2H5BrO, HNO3:H3PO4) prior to CdCl₂ treatment. The CdCl₂ treatment has been found effective in reduction of sheet resistance. Some of the case studies have shown us the effectiveness of proper Cu doping in back contact region gifting adequate hole density, improved life time and good collection of carriers [IV-VI].

II. Theoretical Background for analysis

The total photo generated current, I_{ph} , due to drift of the carrier is given by [XXIII]

$$I = qA \left[\frac{L_h}{\tau_h} p_{NO} + \frac{L_s}{\tau_s} n_{PO} \right] (e^{qV/k_B T} - 1) - qAG(L_h + L_s) \quad (1)$$

Where $I_{ph} = qAG(L_h + L_s)$, the photo generated current and

$$I_s = qA \left[\frac{L_h}{\tau_h} p_{NO} + \frac{L_s}{\tau_s} n_{PO} \right] \quad (2)$$

For short-circuited diode, $V=0$, and $I_{sc} = I_{ph} = qAG(L_h + L_s)$ (3)

For open-circuited diode, $I=0$, and $V = V_{oc} =$

$$\frac{k_B T}{q} \ln \left[\frac{L_h + L_s}{\left(\frac{L_h}{\tau_h} p_{NO} + \frac{L_s}{\tau_s} n_{PO} \right) G + 1} G + 1 \right] = \frac{k_B T}{q} \ln \left[\frac{I_{ph}}{I_s} + 1 \right] \quad (4)$$

Under illumination, the output power is given by [XXIII]

$$P = IV = I_s V (e^{qV/k_B T} - 1) - I_{ph} V \quad (5)$$

Where $V = \frac{k_B T}{q} \ln \left[\frac{1 + I_{ph}/I_s}{1 + qV/k_B T} \right]$, for maximum power output $P_m = V_m I_m$, where

$$V_m = \frac{k_B T}{q} \ln \left[\frac{1 + \frac{I_{ph}}{I_s}}{1 + \frac{qV_m}{k_B T}} \right] =$$

$$V_{oc} - \frac{k_B T}{q} \ln \left[1 + \frac{qV_m}{k_B T} \right] \text{ and } I_m \cong I_{ph} \left[1 - \frac{1}{qV_m/k_B T} \right] \quad (6)$$

The conversion efficiency, $\eta = \frac{P_m}{P_{in}}$, where P_{in} is the incident power. To maximize the output power, both I_{sc} and V_{oc} must be large [XXIII]. The term fill factor is used to define the power extraction efficiency and is expressed as

Fill Factor (FF) = $\frac{I_m V_m}{I_{sc} V_{oc}}$, the important figure of merit of solar cell design (7)

In the time of illumination of a solar cell, photo generations and recombination of minority carriers happen. The following equation explains the steady state of minority carrier diffusion.

$$D_n \left[\frac{\partial^2 (n_p - n_{p0})}{\partial x^2} + G(x) - \frac{(n_p - n_{p0})}{\tau_n} \right] = 0 \text{ and}$$

$$L_n^2 = D_n \tau_n \quad (8)$$

where, L_n or L_e , diffusion length of the minority carriers; D_n , diffusion coefficient, $G(x)$, recombination rate; τ_n , lifetime; $(n_p - n_{p0})$, the excess minority carriers density. The contact barrier height, Φ_b , for holes at the metal/semiconductor interface when the Fermi level is not pinned by interface states [XXIII].

$$\phi_b = \frac{E_g}{q} + \chi - \varphi_m \quad (9)$$

$$\begin{aligned} \phi_i &= \chi + \frac{E_C - E_{Fp}}{q} - \varphi_m \\ &= \varphi_s - \varphi_m = \phi_b - kT \ln \left(\frac{N_V}{N_A} \right) \end{aligned} \quad (10)$$

$$x_d = \sqrt{\frac{2E_s \phi_i}{qN_A}} \quad (11)$$

Where E_g is the band gap, E_V stands for valance band, E_F Fermi level, E_C conduction band, χ is electron affinity of p-type CdTe, E_{Fp} .fermi level near valance band, ϕ_i built in potential for the barrier and φ_m is work function of the back contact metal. At the CdTe/metal interface, the hole current can be written as

$$J_h = -J_{ho} \left(e^{\frac{qV_b}{kT}} - 1 \right) \quad (12)$$

The CdTe/metal junction is opposite that of the main junction, and hence the negative sign convention for its current. In Eq.11, q is electronic charge, k is Boltzmann constant, T is temperature in Kelvin, V_b is the voltage across back contact, and the back contact saturation current J_{ho} can be expressed as [XXIII]

$$J_{ho} = qV_R N_v e^{-q\phi_b/kT} \quad (13)$$

Where N_v is effective density of states in the E_v , Richardson velocity, V_R is the thermal velocity is $3e7$ cm/sec [XXIII]

The current that flows through the back contact is

$$J_h = -J_{ho} \left(e^{\frac{qV_b}{kT}} - 1 \right) + \frac{V_b}{R_{sh}} \quad (14)$$

Where V_b is the voltage across the back contact junction and R_{sh} is the shunt resistance [XXIII]. At $R_{sh} = \infty$, the rollover exists significantly with a flat response. With the decreasing of R_{sh} , when it be equal to R_s , the series resistance, the rollover disappears despite of existence of barrier height in the metal semiconductor junction.

Maximum electric field [XXIII]

$$\mathbf{E} = -\frac{q}{\epsilon} N_d x_{n_0} = -\frac{q}{\epsilon} N_a x_{p_0} \quad (15)$$

Contact potential [XXIII] $V_0 = \frac{kT}{q} \ln \left(\frac{N_a N_d}{n_{ip} n_{in}} \right)$ (16)

Width of the barrier [XVIII]

$$d = (N_a + N_d) \sqrt{\frac{2V_0 \epsilon_0 k_n k_p}{q N_a N_d (k_p N_a + k_n N_d)}} \quad (17)$$

Where N_a the acceptor concentration of p is type and N_d is the donor concentration of n type.

III. Modeling and Simulation

In solar cell, the photons create electron-hole pairs (EHPs) which are forced to reach terminals by the electric field of the junction. Depending upon the band profile at the junction and some other related transport parameters like recombination loss and life time of carriers, conversion efficiency and overall performance mainly occur. The basic semiconductor transport equations involving the continuity equation, Poisson equation and current equations are to be used with proper care of generation-recombination processes to solve the numerical equations for our simulation work. . We use the fluorine doped SnO₂ as the transparent conducting oxide (TCO) layer [XVI, XXII, XXV]. AM 1.5 G radiation standard has been used for all simulation work, while rest of other simulation parameters are furnished in Table 1.

The schematic model of simulated device fabrication is shown in figure 1. The figure describes the simulated structure of our proposed model. Solar radiation clearly passes through the top glass material and entered through the transparent conducting oxide (TCO) at window layer. The radiation then works at the junction of the n-CdS and p-CdTe layer. The back surface field makes the schottky barrier narrower that enhances tunnelling of holes. The model considers the back contact Schottky barrier to investigate the effect of it on the cell..

We consider experimental data in refs. [III, X, XIII, XVI] have been furnished in the following tabular forms and also from some other referred journals sited in this paper. Standard barrier heights like 0.4 eV, 0.5 eV and 0.6 eV, have been chosen for the work as for CdTe/metal contact [VII, IX, XVII, XX-XXI]

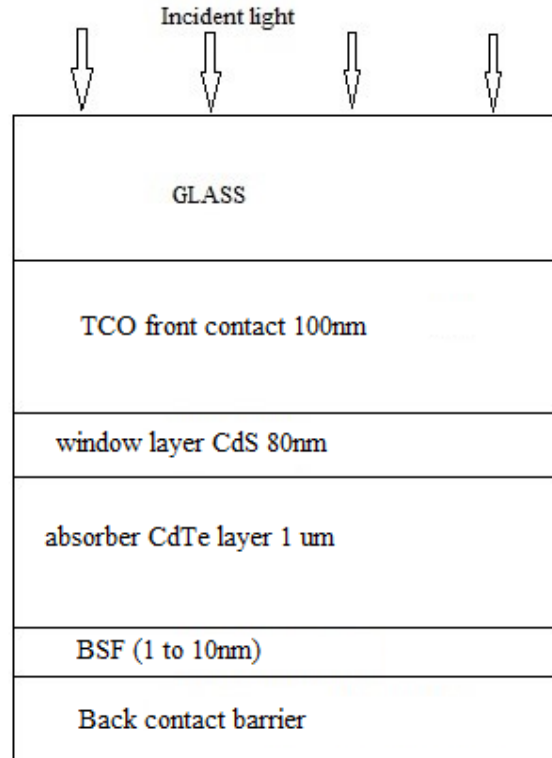
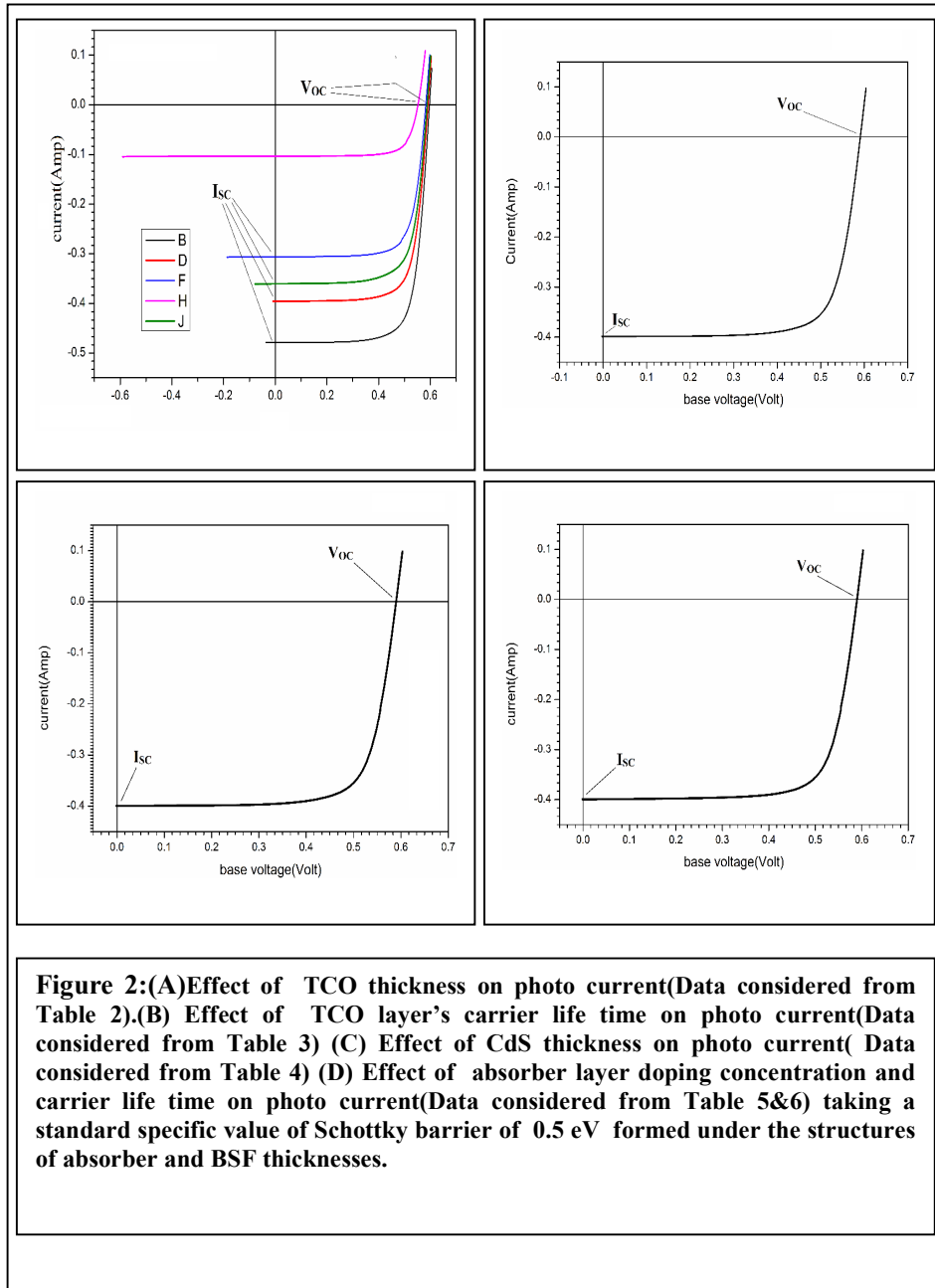


Figure 1: Schematic structure of the CdS/CdTe solar cell

IV. Results and Discussion

All the relevant simulation parameters have been furnished in table 1 accordingly. Figure 2 A shows the voltage-current characteristics of the solar cell. The cell has been simulated under different thicknesses of transparent conducting oxide (TCO) layer thicknesses. Cadmium telluride (CdTe) solar cells have always been standardized by 100 nanometer (nm) TCO layer thickness. However in our work we have achieved most significant performance for 0.09 micrometer (μm) TCO thickness. The simulation results have been furnished in table 2. We observed that for changing thicknesses, short circuit current (I_{sc}) changes. But have got almost constant open circuit voltage (V_{oc}). We also investigated the effect of career lifetime of the TCO layer. The results are furnished in table 3. Here we observe that $4.28 \times 10^{-5} \mu\text{s}$ career lifetime gives the best performance in terms of short circuit current and efficiency (η). This best result has been furnished in figure 2B. As we usually consider the TCO with high doping concentration, very thin layer of it can exhibit good performance with little shorter career life time. Figure 2C depicts the optimum result of CdS thickness. The simulated data of the figure have been provided in table 4. The $0.079 \mu\text{m}$ is seen the best to provide good performance. More thinning of CdS layer experiences pinhole effect that might affect the cell performance. So very thin CdS layer (less than 80nm) is not advisable for designing better solar cell. The investigations on pinhole are excluded in this work. Our next investigation was for observer layer. We use cadmium telluride as the observer layer. We considered $1 \mu\text{m}$

slandered thickness for our work. Here we investigated absorber layer with varied doping concentration and carrier lifetime. Higher carrier lifetime and doping concentration have been more suggestible to design a better solar cell. The simulated results are given in Table 5 and 6.



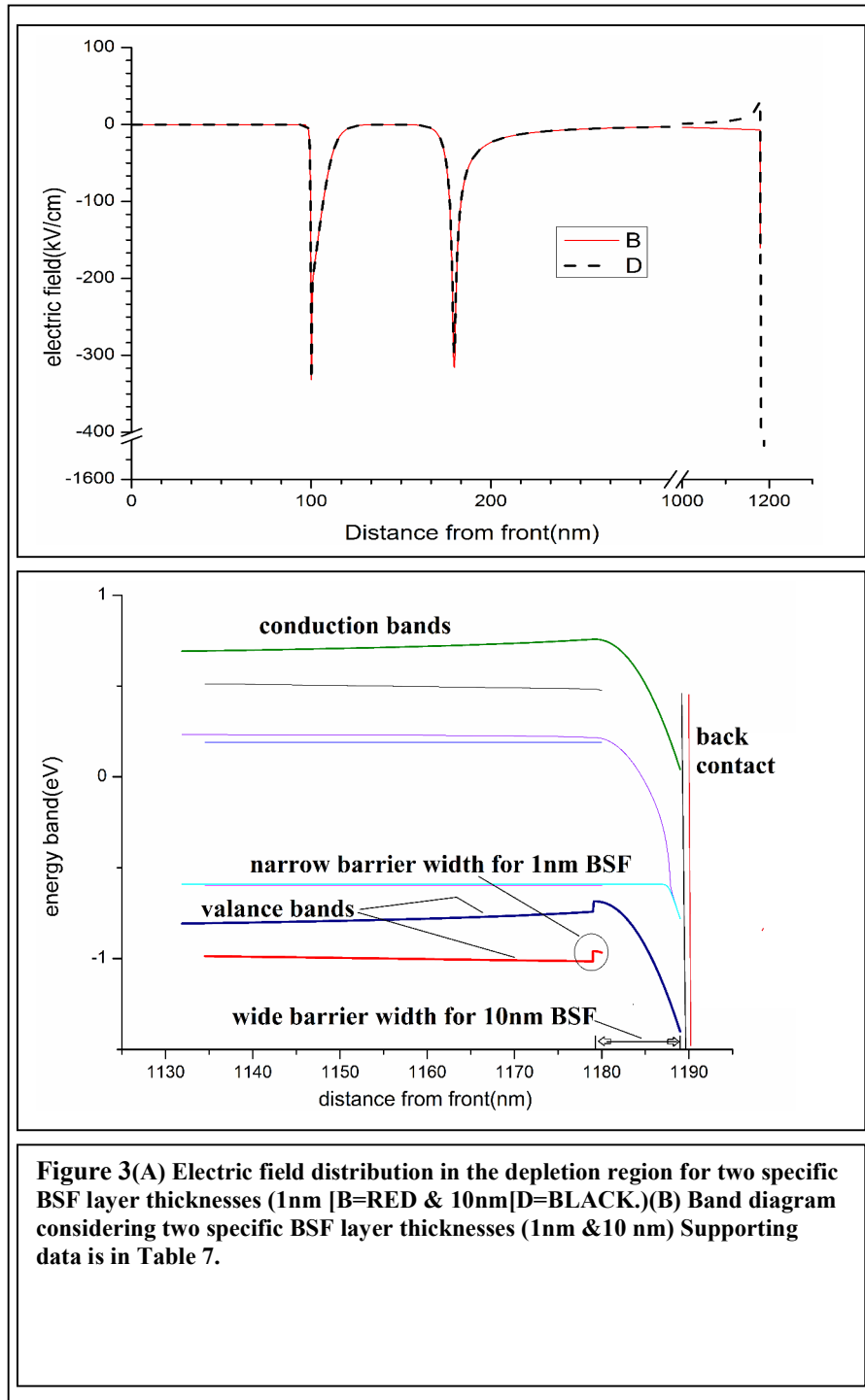


Table1: Input parameters

sample	Doping concentration	Bulk recombination	Thickness
SnO ₂	1e20cm ⁻³	1ns	100nm
CdS	1e18cm ⁻³	80ns	79-200nm
CdTe	1e14cm ⁻³	1ns	1μm
BSF	7e18cm ⁻³	1ns	1-10nm

Table 2: Simulated data for Fig.2 A

Thickness (μm)	I _{sc} (Amp)	V _{oc} (Volt)	η _i (%)	FF (%)	curve
0.2	0.104	0.5523	4.31	75	H
0.13	0.3062	0.5826	13.45	75.4	F
0.1	0.3957	0.591	17.62	75.34	D
0.09	0.4788	0.5969	21.52	76	B
0.03	0.3605	0.587	15.59	73.37	J

Table 3: Simulated data for Fig.2 B

Carrier Life time	V _{oc} (Volt)	I _{sc} (Amp)	η _i (%)
5.00E-05	0.586014	-	14.7359
4.90E-05	0.586487	-	14.9906
4.80E-05	0.587018	-	15.2806
4.70E-05	0.587616	-	15.6141
4.60E-05	0.588294	-	16
4.50E-05	0.589067	-	16.451
4.40E-05	0.589956	-	16.9839
4.30E-05	0.590987	-	17.6214
4.29E-05	0.591099	-	17.692
4.28E-05	0.591213	-0.3987	17.7632

Table4: Simulated data for Fig.2 C

Thickness (μm)	Voc (Volt)	Isc (Amp)	η(%)
0.084	0.5923	-0.3961	17.730
0.083	0.5920	-0.3967	17.735
0.082	0.5918	-0.3973	17.75
0.081	0.5916	-0.3980	17.760
0.08	0.5912	-0.3987	17.763
0.079	0.59	-0.3994	17.78

Table 5: Simulated data for Fig.2 D

Doping (cm ⁻³)	Voc (Volt)	Isc (Amp)	η(%)
1.00E+14	0.59	-0.3987	17.6
5.00E+15	0.59	-0.399	17.78
1.00E+16	0.5898	-0.399	17.84

Table 6: Simulated data for Fig.2 D

Carrier life Time(μs)	Voc (Volt)	Isc (Amp)	η(%)
0.001	0.589851	-0.399	17.6968
0.002	0.589904	-0.39925	17.7264
0.003	0.589928	-0.39933	17.7486
0.004	0.589943	-0.39938	17.76
0.005	0.589953	-0.39941	17.78

Table 7: Simulated data for Fig. 3 A & B

BSF Thickness (μm)	Contact Barrier (eV)	Isc (Amp)	Voc (Volt)	η(%)
0.01	0.4	0.3992	0.5904	18.30
0.01	0.5	0.3994	0.59	17.78
0.01	0.6	0.3983	0.5895	14.97
0.001	0.4	0.3907	0.5898	17.55
0.001	0.5	0.3906	0.5898	17.53
0.001	0.6	0.411	0.591	18.39

So we achieved so far the best efficiency for $1e16\text{cm}^{-3}$ doping concentration and $0.005\mu\text{s}$ carrier life time of CdTe absorber layer. The V-I curve for this better result is shown in figure2D.

We also had investigations for back surface field thickness optimization with varied schottky barrier height. Here we considered 0.4, 0.5 and 0.6 electron volt (eV) as the standard back contact barrier heights for cadmium telluride solar cell. Through the investigation, we achieved very important and significant information regarding the consideration of BSF thickness and back contact barrier height. The simulation results have been furnished in table 7. The corresponding figures of electric field and band diagram are presented in figure 3A and 3B accordingly. In table 7, we observed that thicker BSF layer is better for lower schottky height whereas very thin BSF layer is better for higher schottky barrier heights. Figure 3 A shows us an electric field distribution at 0.6 eV schottky barrier for two specific BSF thicknesses. For very thin BSF layer (1nm), the electric field at the schottky contact is depleted in a better way with respect to thicker (10nm) BSF layer. For this reason, we observe in figure 3B that 1nm BSF experiences narrow barrier width where 10 nm BSF layer provides wider schottky barrier that restricts tunneling of majority carriers. So our investigation suggests thinner BSF layer for higher schottky heights.

V. Conclusion

Open circuit voltages (V_{OC}) were almost constant during investigations. We achieved the good efficiency (17.78%) with a standard Schottky barrier height (0.5 eV). Thinning of BSF layer has been significant to work better against higher Schottky barrier. In addition, higher carrier life time and doping concentration of absorber layer are advisable for efficient cell design. The insertion of the very thin BSF layer has been a good alternative to enhance the performance of the cell against higher the back contact schottky barrier. Basically it makes the barrier width narrower that promotes more holes tunnelling along with reflecting the electrons resulting good performance. During the investigation on TCO and CdS layer thicknesses we realised that, beyond a limit, thinning of the layers may give rise to defects like pinhole formation and Fermi level pinning that can affect the cell performance. A further scope of work is thereby generated in this direction to tune the Fermi level and to prevent the pinhole effect.

Acknowledgement

The authors would like to acknowledge the R & D cell of the University of Engineering & Management, Kolkata, India for the cooperation and advice extended.

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