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OPTICAL PARALLEL HALF ADDER USING SEMICONDUCTOR OPTICAL AMPLIFIER-ASSISTED SAGNAC GATES

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Abstract

In Today communication needs huge operational speed. This will be accomplished in case the conventional carrier of data, i.e. electron is supplanted by a photon for gadgets based on switching and logic. Gates are the basic building pieces of advanced frameworks. Different logic and arithmetic operations can be done using this gate. Optical logic and arithmetic operations are exceptionally much anticipated in high-speed communication frameworks. In this paper, we have presented parallel models to perform the addition of two binary digits based on terahertz optical asymmetric demultiplexer (TOAD)/semiconductor optical amplifier (SOA)-assisted Sagnac gates. Using only two TOAD-based switches we have designed a parallel half adder. This optical circuit increases the speed of calculation and is also capable of synthesizing light as an input to form the output. The most advantage of this parallel circuit is that no synchronization is required for distinctive inputs. The circuit is hypothetically planned and confirmed by numerical simulations.

Keywords: Terahertz optical asymmetric demultiplexer; semiconductor optical amplifier; half adder; optical logic.

I. Introduction

Now a day's high-speed all-optical logic gates are very important devices in optical networks because they perform the necessary signal processing functions such as switching regeneration and recognition processing on photonic switching nodes [II, VII XII]. A revolution has been brought in the all-optical data processing system. Among the various optical switches, the Sagnac Gate with Terehartz Optical Asymmetric Demultiplexer (TOAD) / Semiconductor Optical Amplifier (SOA) effectively combines low power consumption, high repetition rate, and fast switching time [I, XIV, XV]. Different types of adder utilizing the SOA-assisted Sagnac interferometer have been proposed and illustrated by different research groups [V, VI, VIII, IX, X]. A modern strategy of applying optical frequency encoded operations utilizing Mach-Zehnder interferometer in expansion to SOA by Ghosh et al [IV]. In this paper optical parallel half adder utilizing TOAD-based switches has been designed. Both the ports reflected and transmitted are used to design the circuit.

II. Architecture of TOAD based switch

The Basic architecture of TOAD based switch is appeared in Fig. 1 [XI, XIII]. Here a nonlinear component (NLE) is set unevenly in a circle. The NLE is a semiconductor optical enhancer. In this paper, we have attempted to utilize the yield from both the transmitting and reflecting modes. The control at upper and lower can be written as [III, XIV, XV].

$$P_{Upper}(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) - 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \quad (1)$$

$$P_{Lower}(t) = \frac{P_{in}(t)}{4} \cdot \left\{ G_{cw}(t) + G_{ccw}(t) + 2\sqrt{G_{cw}(t) \cdot G_{ccw}(t)} \cdot \cos(\Delta\varphi) \right\} \quad (2)$$

where $G_{cw}(t), G_{ccw}(t)$ is the power gain. The time-dependent stage contrast between clockwise and counter-clockwise beats is $\Delta\varphi = -\alpha/2.\ \ln\left(G_{cw}(t)/G_{ccw}(t)\right)$ with α being the line-width improvement figure.

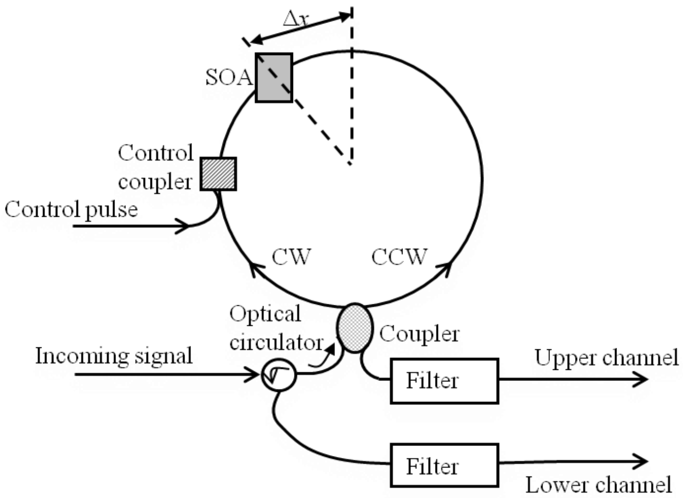

Fig. 1. A TOAD based optical switch with single control pulse.

Absence of a control, information enters the fiber circle, passes through the SOA at distinctive times as they counter-propagate around the circle and involvement the same unsaturated gain and recombine at the input coupler i.e. $G_{ccw} \approx G_{cw}$. At that point, $\Delta\varphi \approx 0$ and expression for and $P_{Lower}(t) = P_{in}(t) \cdot G_{ss}$. It appears that information is reflected back toward the source. When a controlled beat is infused into the circle, it soaks the SOA and changes its file of refraction. The pickup of SOA diminishes quickly. As a result, the two counter propagation information will involve differential pick-up immersion profiles. Hence they recombine at the input coupler, then the information will exit from the upper port i.e., $P_{Upper}(t) \neq 0$ and $P_{Lower}(t) \approx 0$, the comparing values can be gotten from the equation (2). A channel may be utilized at the yield of TOAD based switch to dismiss the control and pass the approaching pulse. Fig. 2 shows the corresponding diagram of TOAD based switch.

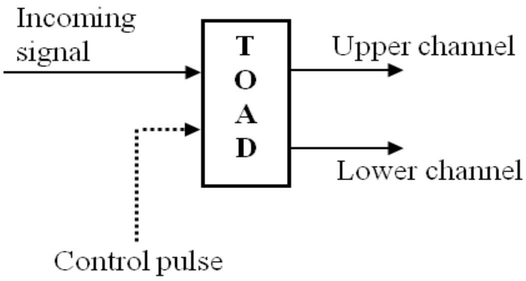

Fig. 2. The diagram of TOAD based switch.

III. Optical parallel half adder

A half adder takes the two inputs as two binary numbers viz., A and B and produces the output as a sum (S) and a carry (Cout). Both the sum (S) and carry (Cout) are one bit. The circuit diagram of the optical parallel half adder is shown in Fig. 3. To design this circuit, we use only two TOAD-based switches namely, TOAD1 and TOAD2.

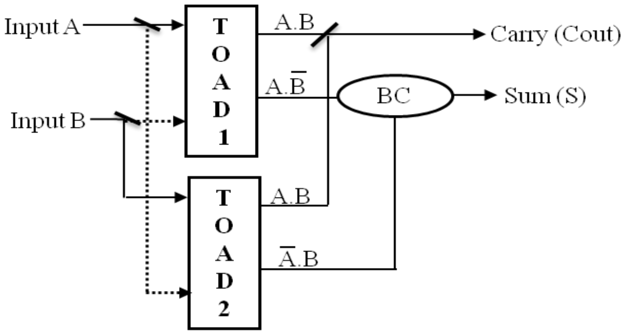

Fig. 3. Diagram of an optical parallel half adder, where A and B: Inputs, BC: Beam combiner, /: Beam splitter and Sum and Cout: Final outputs.

Input A and input B are the light source. The presence of light is in one state and the absence of light is in zero states. When input A = B = 0, then no light incident on the switches so both the switches become inactive hence sum (S) = 0 and a carry (Cout) = 0. If input A = 1 and input B = 0 then only switch TOAD1 become active and light follow the lower channel of TOAD1 so sum (S) = 1 and a carry (Cout) = 0. Similarly, if input A = 0 and input B =1 then only switch TOAD2 becomes active and light follows the lower channel of TOAD2 so sum (S) = 1 and a carry (Cout) = 0. When input A = B = 1, then light incident on the switches so both the switches become active hence sum (S) = 1 and a carry (Cout) = 1. All the operations verify as a half adder.

IV. Results and Discussions

The parameters utilized in this paper are taken from the writing overview of distinctive investigate papers [III, XIV, XV]. The values of diverse parameters as : unsaturated enhancer pick up of the SOA (G_{ss}) = 20 dB, pick up recuperation time of SOA (τ_e) = 100 ps, the exchanging beat vitality E_{cp} = 100 fJ, immersion vitality of the SOA (E_{sat}) = 1000 fJ, the unpredictability of the circle (T_{asym}) = 30 ps, line-width upgrade calculate (α) = 6, full width at half greatest of control beat (σ) = 12 ps, and bit period (T_c) = 50 ps, so that the operational conditions are fulfilled. The corresponding input and output waveforms of the adder circuit are shown in Fig. 4 and Fig. 5, respectively.

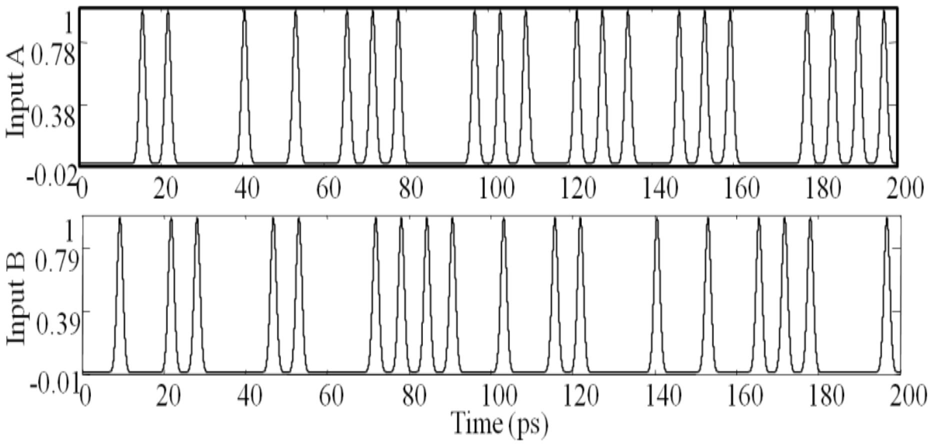

Fig. 4. Input waveforms of Input A and Input B.

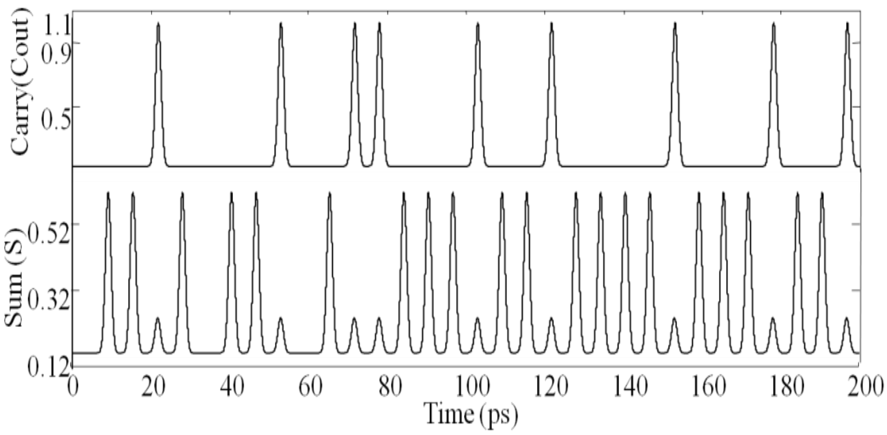

Fig. 5. Output waveforms of the Sum (S) and Carry (Cout).

To study the function of the circuit, we find the appropriate value of the SOA short signal gain for which the switching power is reduced. For this reason, the dependence of the switching power on the small-signal gain is plotted in Fig. 6. From this figure, it can be seen that the power decreases significantly with the increase of the small-signal gain and reaches a minimum of 100 fJ at 20 dB.

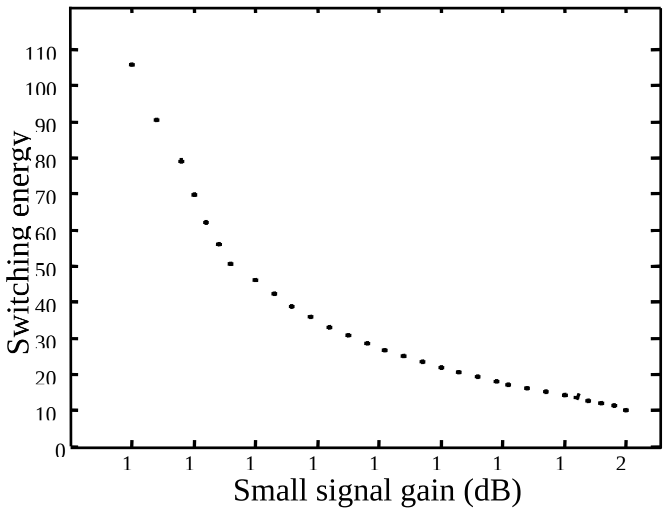

Fig. 6. Switching energy variation with respect to small signal gain.

V. Conclusion

We have designed optical parallel half adder utilizing only two TOAD-based switches. The circuit has been designed theoretically and verified through numerical simulation. Both the ports reflected and transmitted are used to perform the simulation of the circuit. This circuit gives the desired result at the outputs. This circuit can be used as a basic building block to design complex circuits.

Conflicts of Interest:

There is no conflict of interest regarding the paper.

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