



## All-Optical Logic Gates Based on Graphene Interferometric Waveguide

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### Abstract

*Novel types of all-optical logic gates based on graphene surface plasmonpolaritons (SSPs) are proposed in this study by utilizing linear constructive and destructive interferences among SSP waves in spatially separated graphene sheets. The realized logic gates are OR, AND, and XOR gates. The suggested transmission value threshold between the two states logic 0 and logic 1 is 0.5. Small modification in the structure has been conducted to implement the XOR gate with the same wavelength for all the proposed gates. The structure performance is measured on the basis of transmission efficiency of each implemented gate. The state of each input port can be easily controlled by switching the external gate voltage either ON or OFF. The function of the proposed gates can be achieved by modifying the chemical potential ( $\mu_c$ ), coupling length ( $L_c$ ), or inter spacing among the graphene sheets ( $d$ ). These compact-sized logic gates are considered an important part in the integration of nanoscale photonic devices.*

**Keywords :** Graphene, Surface plasmonpolaritons (SPPs), All-optical logic gate, Nanophotonic devices, Plasmonic logic gates.

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### I. Introduction

Graphene, as a new material type, has attracted considerable attention, especially in the research fields that focus on optoelectronics and other applications, due to its ideal properties [I]. The carrier mobility of graphene is approximately  $2 \times 10^5 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ , which allows fabrication of ultra speed photonic components [II]. The episode light can be coupled firmly to graphene plates and afterward energize the graphene surface plasmonpolaritons (SPPs) over the surface of input ports [III-V].

The SPPs are the aggregate motion conduct of the free electrons on the material surface energized by outer sources. Owing to the remarkable specifications of SPPs, different types of sub wavelength photonic components have been scrutinized because these components can overcome the diffraction limit problem [VI, VII]. Traditional electronic logic gates have been imperative parts in signal processing and transmission systems. In any case, these gates have demonstrated a few drawbacks in various applications, such as latency failure, which decrease the reliability of devices. Nevertheless, all-optical logic gates can adapt to deformities, thereby attracting considerable attention [VIII-X]. Many all-optical gates can be actualized; several of them depend on optical interface [I, III-VIII], whereas others depend on nonlinear effects [IX-XII]. In Ref. [XIII], the cascaded gates in nanoscale photonic plasmon devices are exhibited, and the authors presume that the plasmonic NOR gate can be executed by utilizing cascaded OR and NOT logic gates. In Ref. [XIV], all-optical XOR, XNOR, and NOT gates in nanoscales are executed by utilizing plasmonic waveguides dependent on the linear interface among SSP modes. In Ref. [XV], the authors explore the optical properties of the graphene material depending on plasmonic waveguide that acts as AND and OR gates. Motivated by the recorded results of structured gates, the constructive or destructive coupling behavior will be utilized to realize different types of GSP-based logic gates. This article is organized as follows. The first part presents a concise introduction. The second part discusses the structure of the gates and the essential properties of graphene material. The third part comprehensively explores the different types of logic gates. The fourth part provides the conclusion.

## II. Geometric structure and basic concepts

Considering the SPP coupling hypothesis of the graphene waveguide design shown in Fig. 1 and explored in [XVI], the SPP coupling coefficient ( $C_g$ ) among the graphene ports can be obtained as follows [XVII, XVIII]:

$$C_g = \frac{\beta_- - \beta_+}{2} \quad (1)$$

The coefficient of propagation constant ( $\beta_+$ ) is given as

$$\beta_{\pm} \approx k_{SPP} + \frac{2i \varepsilon_h k_0 / (\eta_0 \sigma_g) - k_p (1 \mp u_p)}{(1 \mp u_p) k_{SPP} / k_p \pm k_{SPP} d} \quad (2)$$

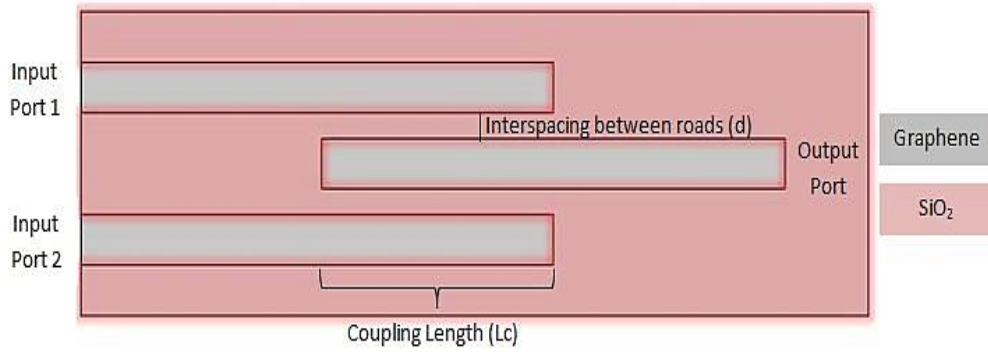
where  $k_p = (k_{SPP}^2 - \varepsilon_h k_0^2)^{\frac{1}{2}}$ , and  $u_p = \exp(-k_p d)$  [XVII].  $\varepsilon_h$  is the dielectric permittivity of the channel where the isolated graphene layers are implanted,  $d$  is the space among the plates of graphene,  $\sigma_g$  is the surface conductivity of graphene,  $\eta_0 = 377\Omega$  (this value represents air impedance),  $k_0 = 2\pi / \lambda_0$  ( $\lambda_0$  is the wavelength of the episode light in air), and  $k_{SPP} = k_0 \left[ \varepsilon_h - 4\varepsilon_h^2 / (\eta_0 \sigma_g)^2 \right]$  is the wave vector of SPPs supported by a graphene with a single layer [XVI]. The graphene material is usually represented as a two-dimensional material, and its tunability is

based on the complex surface conductivity, which is reduplicated by the intraband and interband contribution transitions [XIX] as  $\sigma = \sigma_{\text{intra}} + \sigma_{\text{inter}}$ . The two terms can respectively be represented as

$$\sigma_{\text{intra}}(\omega) = \frac{ie^2\mu_c}{\pi\hbar^2(\omega + i\tau^{-1})}, \quad (3)$$

$$\sigma_{\text{inter}}(\omega) = \frac{ie^2}{\pi\hbar^2} \ln \left( \frac{2|\mu_c| - (\omega + i\tau^{-1})\hbar}{2|\mu_c| + (\omega + i\tau^{-1})\hbar} \right). \quad (4)$$

The conditions over (3) and (4) are legitimate only when  $k_B T \ll |\mu_c|$ .  $\hbar$  represents the reduced Planck's constant,  $e$  is the electron charge,  $\mu_c$  is the chemical potential,  $\tau$  is the relaxation time constant,  $\omega$  is the radian angular frequency,  $T$  is the temperature in Kelvin, and  $k_B$  is the Boltzmann constant [XX].



**Fig. 1. Graphene waveguide configuration**

The coupling coefficient  $C_g$ , which is given in Eq. (1), can determine the coupling length  $L_c$  that gives the total mode propagated distance until the total energy is transferred from one waveguide to another, as given by [XVI, XXI]

$$L_c = \frac{\pi}{2\sqrt{2}|C_g|} \quad (5)$$

### III. All-Optical Logic Gates

The functions of the proposed gates can be realized by the constructive and destructive interferences between the input signals from the two input ports. For example, when input port 1 is disabled (OFF state) and input port 2 is active in (ON state) or vice versa, the destructive interference occurs between the input signals due to the phase difference that reduces the transmission. When both input ports are active (ON state), the constructive interference occurs between the input signals

[XXII]. In the proposed structure shown in Fig. 1, the graphene thickness is considered fixed with  $\varepsilon_g = 1 + i \sigma_g \eta_0 / (k_0 \Delta)$  [XVI]. The graphene thickness ( $\Delta$ ) is considered = 1 nm to achieve high-speed software processing. Ref. [XX] indicates that the application of an incredibly high electric field is crucial to achieving the relentless task of this structure, which is not the best strategy. In view of Kubo's technique, a reverse connection exists between the applied wavelength and  $\mu_c$ , which is the real conductivity (associated with the loss coefficient). In this way, given that the proposed structure requires a low loss waveguide and minimal  $\mu_c$ ,  $10\mu m$  wavelength is applied; this value provides the ideal proportion of mode confinement/losses and enables the structure to work in a low chemical potential ( $\gg 0.25$  eV) [XX].

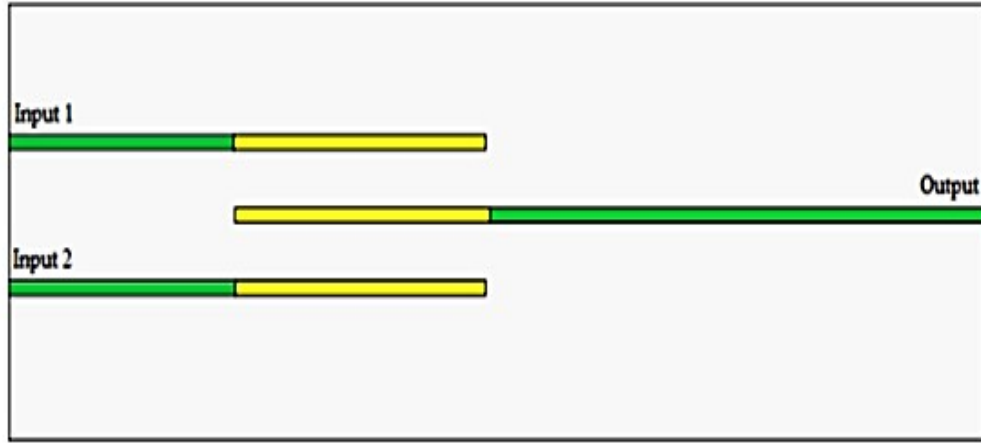


Fig.2. Interferometric device with two inputs and one output

The function of all-optical logic OR gate can be achieved from the proposed structure as shown above using the following structure parameters:  $L_c = 295.46$  nm,  $\mu_c = 0.229$  eV,  $d = 52$  nm, and  $\varepsilon_h = 2.1$  (SiO<sub>2</sub> is used as a substraigh).  $\lambda_0 = 10$   $\mu m$ ,  $T = 300$  K, and  $\tau = 0.5$  ps (is rather conservative to feature the practical transport loss of graphene [XVI]).

Fig. 3 shows the SPP distribution in the proposed device for different input states. Figs. 3a, 3b, and 3c show the results when only input port 1 is active (ON state), only input port 2 is active (ON state), and both ports are active (ON state), respectively.

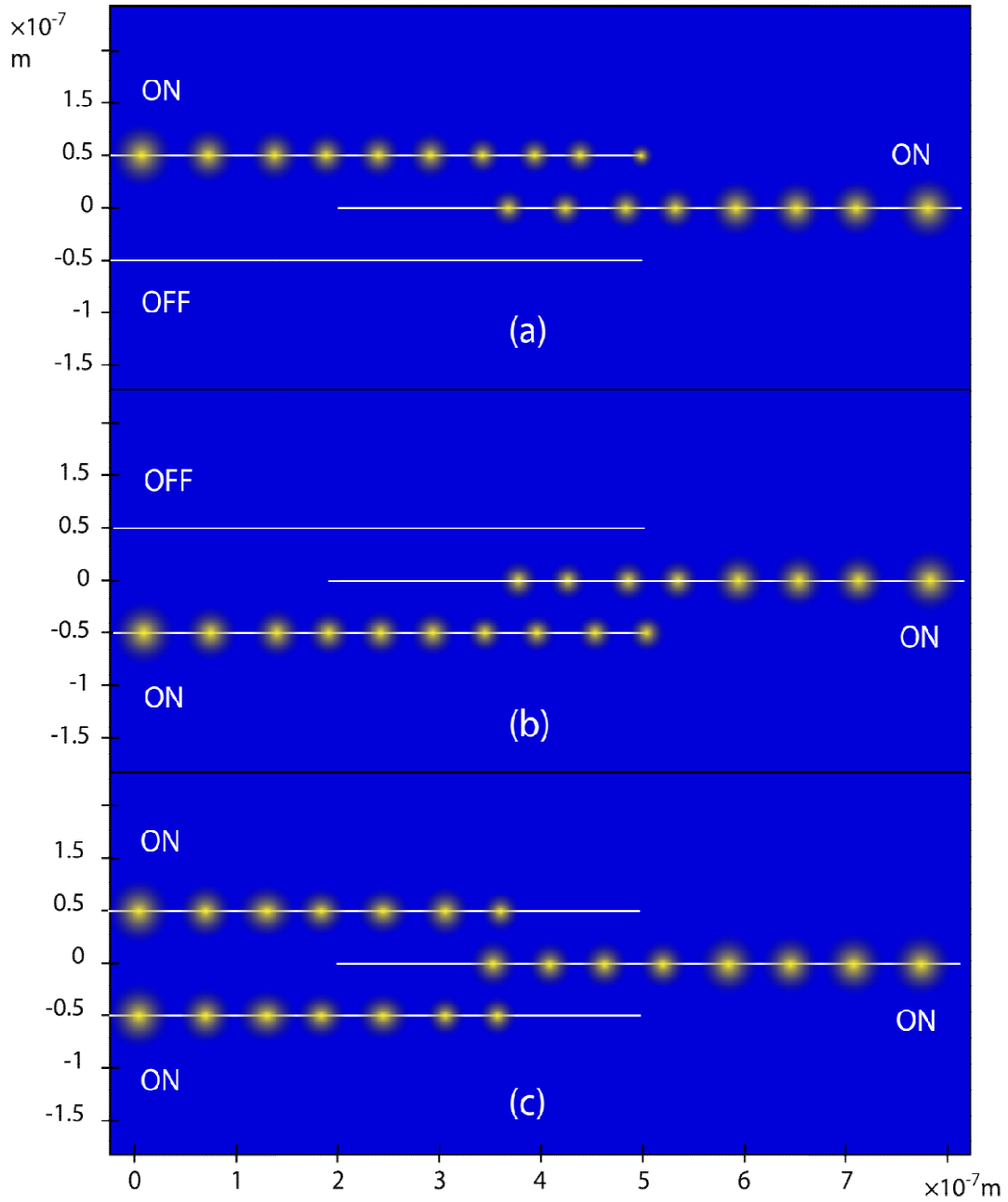
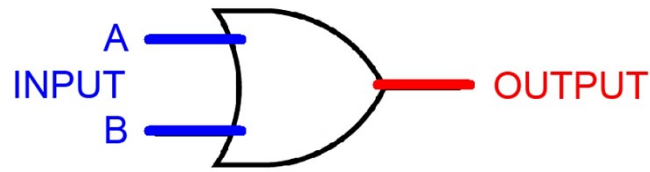


Fig. 3. SPP mode distribution in the structure as logic OR gate with  $\mu_c = 0.229$  eV,  $L_c = 295.46$  nm, and  $d = 52$  nm. Activation input state: (a) only input port 1 is active, (b) only input port 2 is active, and (c) both input ports are active.

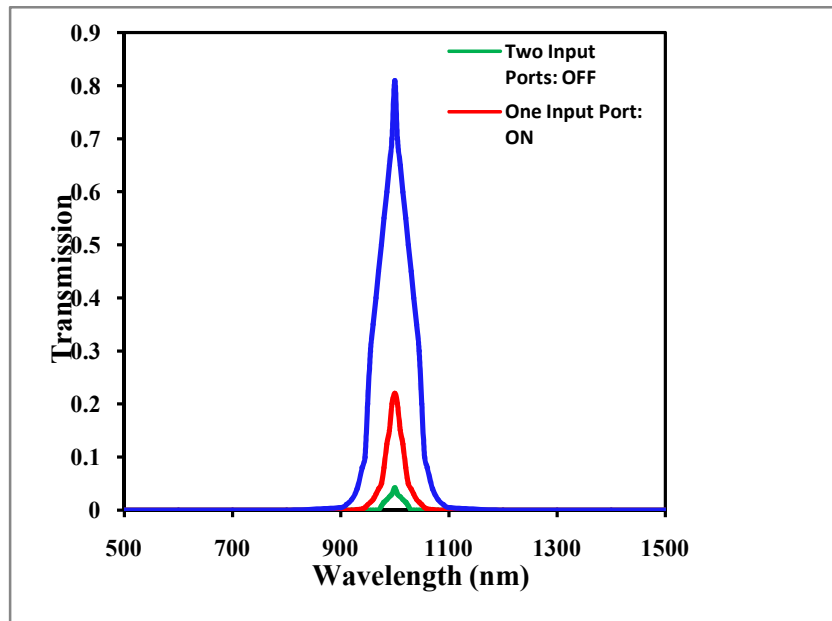
The transmission spectrum of the proposed OR gate structure is shown in Fig. 4c. The operation of the proposed OR gate is summarized in Table 1.



(a)

Input		Output
A	B	$Y=A+B$
0	0	0
0	1	1
1	0	1
1	1	1

(b)



(c)

Fig. 4. (a) Symbol of a traditional electronic OR gate. (b) Truth table of OR gate. (c) Transmission efficiency of the proposed all-optical OR logic gate at different input states.

**Table 1** Operation of the proposed OR gate structure.

State of input port 1	State of input port 2	Activation of input port 1	Activation of input port 2	Transmission efficiency	State of output port	Activation of output port
Logic 0	Logic 0	OFF	OFF	0.42 %	Logic 0	OFF
Logic 0	Logic 1	OFF	ON	22 %	Logic 1	ON
Logic 1	Logic 0	ON	OFF	22 %	Logic 1	ON
Logic 1	Logic 1	ON	ON	81 %	Logic 1	ON

AND logic function can be obtained via the same structure shown in Fig. 1 using the following parameters:  $\mu_c = 0.25$  eV,  $L_c = 409.37$  nm, and  $d = 60$  nm. Fig. 5 shows the electrical field components  $E_y$  and SPP mode distribution in the device for different input logic states. Figs. 5a, 5b, and 5c show the results when only input port 1 is active (ON state), only input port 2 is active (ON state), and both input ports are active (ON state), respectively.

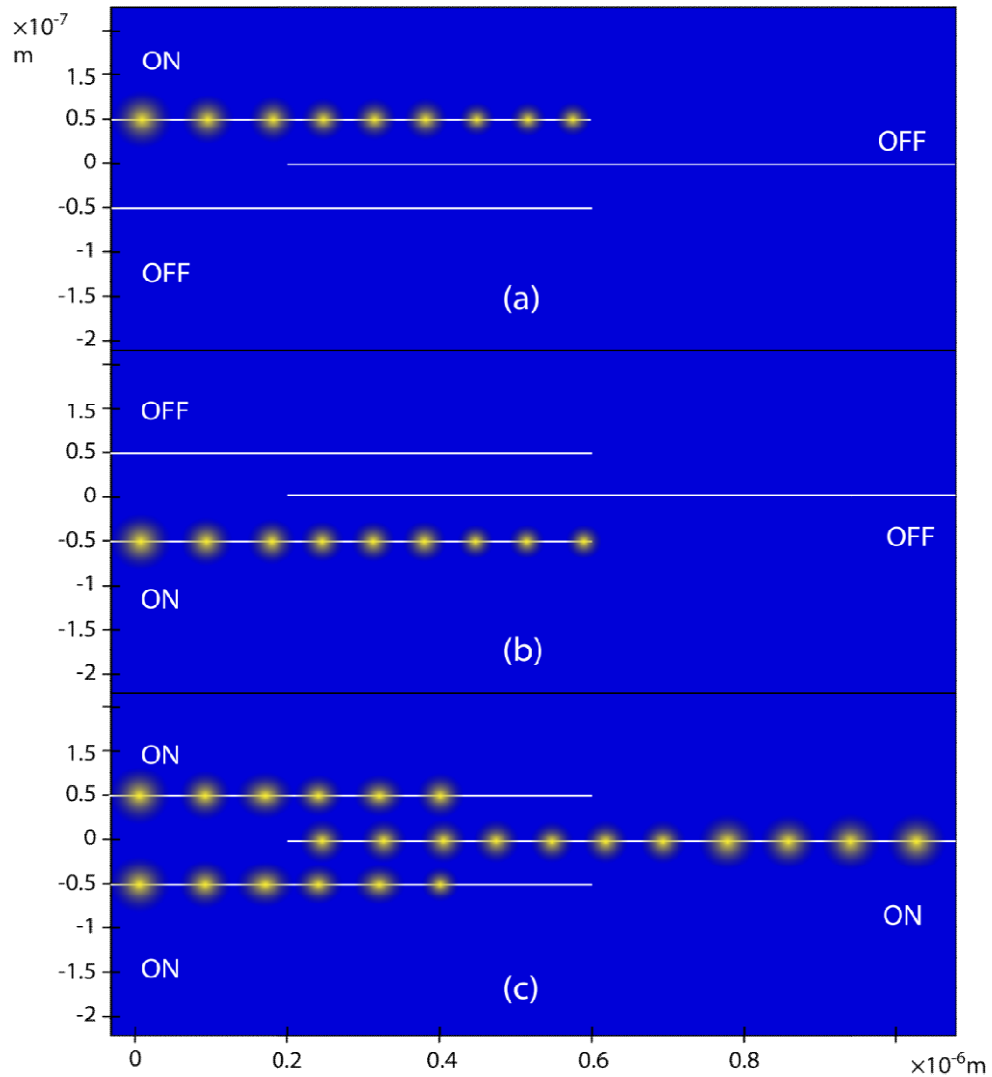
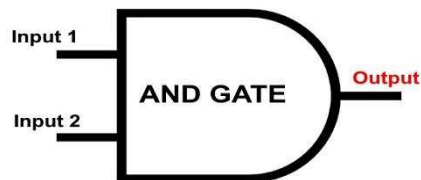


Fig. 5. SPP mode distribution in the structure as AND logic gate with  $\mu_c = 0.25$  eV,  $L_c = 409.37$  nm, and  $d = 60$  nm. Input states: (a) only input port 1 is active, (b) only input port 2 is active, and (c) both input ports are active.

The transmission spectrum of the proposed AND logic gate is shown in Fig. 6c. The operation of the proposed AND gate is summarized in Table 2.

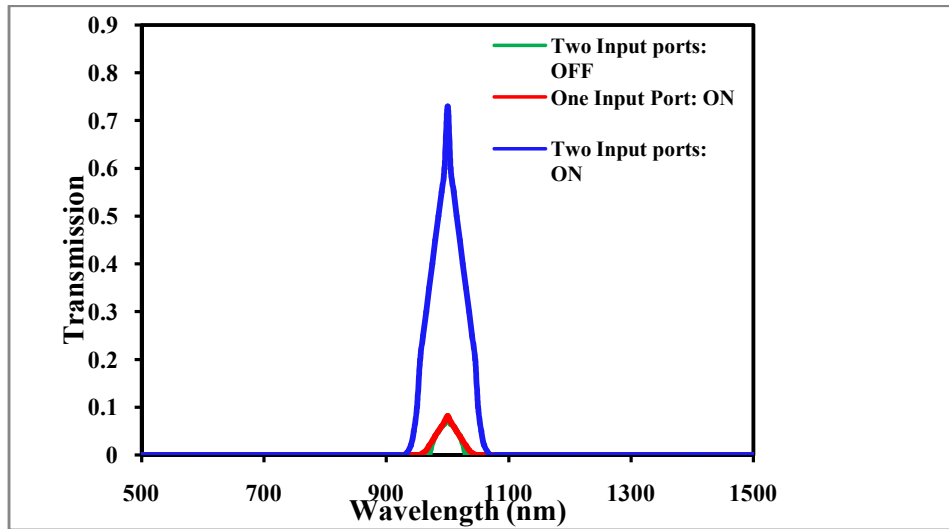


(a)



Input		Output
A	B	$Y=A.B$
0	0	0
0	1	0
1	0	0
1	1	1

(b)



(c)

Fig. 6. (a) Symbol of a traditional electronic AND gate. (b) Truth table of AND gate. (c) Transmission efficiency of the proposed all-optical AND logic gate at different input states.

**Table 2** Operation of the proposed AND gate structure.

State of input port 1	State of input port 2	Activation of input port 1	Activation of input port 2	Transmission efficiency	State of output port	Activation of output port
Logic 0	Logic 0	OFF	OFF	0.73 %	Logic 0	OFF
Logic 0	Logic 1	OFF	ON	0.82 %	Logic 0	OFF
Logic 1	Logic 0	ON	OFF	0.82 %	Logic 0	OFF
Logic 1	Logic 1	ON	ON	73%	Logic 1	ON

The same proposed interferometric structure in Fig. 1 can be used to obtain the function of XOR logic gate by employing the destructive interference between the two input ports caused by slight structure modification in input port 2 [XXIII]. Fig. 7 demonstrates the distinction shape between graphene sheets, which is responsible for the destructive SSP mode coupling when both input ports are active (ON state). The transmission spectrum of the proposed XOR logic gate is shown in Fig. 8c. The operation of the proposed AND gate is summarized in Table 3.

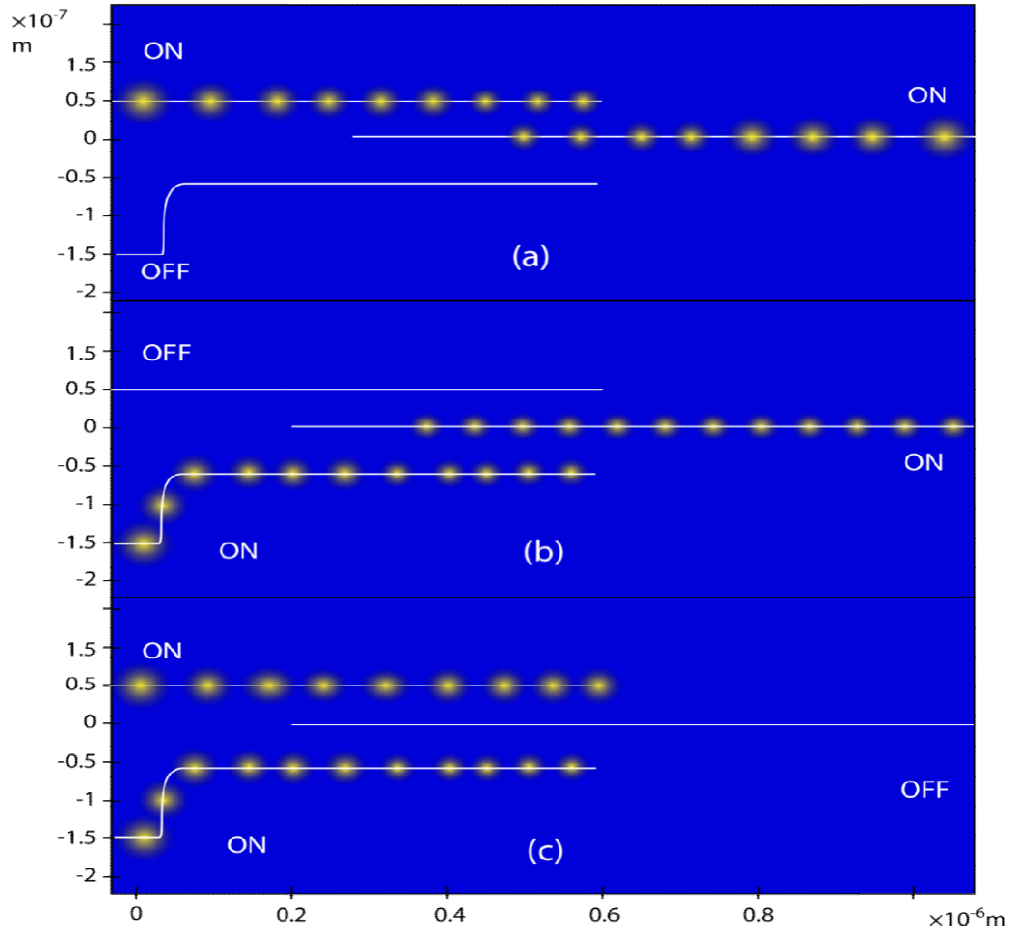


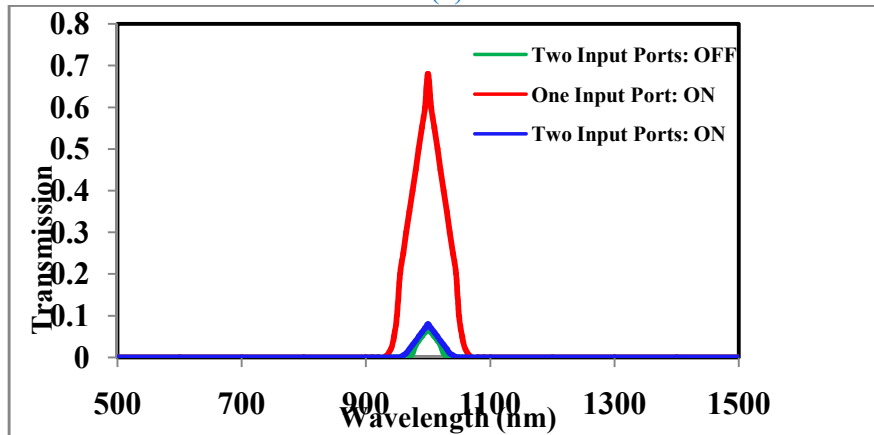
Fig. 7. SPP mode distribution in the structure as XOR logic gate with  $\mu_c = 0.212$  eV,  $L_c = 346.75$  nm, and  $d = 50$  nm. Input states: (a) only input port 1 is active, (b) only input port 2 is active, and (c) both input ports are active.



(a)

Inputs		Output
A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

(b)



(c)

Fig. 8. (a) Symbol of a traditional electronic XOR gate. (b) Truth table of XOR gate. (c) Transmission efficiency of the proposed all-optical XOR logic gate at different input states.

**Table 3** Operation of the proposed XOR gate structure.

State of input port 1	State of input port 2	Activation of input port 1	Activation of input port 2	Transmission efficiency	State of output port	Activation of output port
Logic 0	Logic 0	OFF	OFF	0.65 %	Logic 0	OFF
Logic 0	Logic 1	OFF	ON	68 %	Logic 1	ON
Logic 1	Logic 0	ON	OFF	68 %	Logic 1	ON
Logic 1	Logic 1	ON	ON	8 %	Logic 0	OFF

#### IV. Conclusion

Three all-optical logic gates are proposed and implemented using the gates OR, AND, and XOR in this study. The proposed gates are structured using a graphene interferometric device with two input ports and one output port placed on silica substraight. Utilizing the functions of constructive and destructive interferences among the signals, modifying the coupling length  $L_c$  between the input and output ports with a straight property, changing the interspacing between the ports  $d$ , and

slightly tuning the chemical potential  $\mu_c$  of the plasmonic logic gates are achieved. The state of the output port (0 or 1) is determined on the basis of the transmission value through the port; if the transmission value is above the transmission threshold, which is assumed to be 0.5, then the state is 1; otherwise, the state is 0. Finally, the plasmonic gates are treated as fundamental parts in integrated photonic systems and all-optical signal-processing systems.

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