



## Effects of very thin CdS window layer on CdTe solar cell

Koushik Sarkar<sup>1</sup>, Seerin Jahan<sup>2</sup>, Bhaskar Dutta<sup>3</sup>, Sreelekha Chatterjee<sup>4</sup>  
Souvik Gain<sup>5</sup>, Sreyashi Ghosh<sup>6</sup>

<sup>123456</sup> Future Institute of Engineering and Management, Kolkata-150, India

Corresponding author: Koushik Sarkar: koushik.sarkar@teamfuture.in

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### Abstract

The work is based on the simulation fabrication of a CdS/CdTe thin film solar cell where the benefits and limitations of very thin window (CdS) layer have been investigated. The comparison between with and without pinhole effects for various CdS thicknesses have been analysed. We used highly resistive ZnO layer to overcome the pinhole problem that we had to face due to the consideration of very thin CdS layer to enhance the short circuit current ( $I_{sc}$ ) and open circuit voltage ( $V_{oc}$ ) as well. In this paper, the work is mainly concerned on the degradation of the performance of the solar cell due to pinhole effect and its remedy to enhance the efficiency of the cell. It has been noticed that, the inclusion of a ZnO layer has positive effect on the performance of cell. For very thin CdS layer(50 nm), we observed a poor efficiency of the cell (8.48%) due to pinhole effect. But after insertion of the ZnO layer we recovered the efficiency (19.64%) and overall performance of the cell appreciably.

**Keywords** : CdS, CdTe, pinhole, ZnO

### List of notation

$S_nO_2$	Tin dioxide
TCO	Transparent coating oxide
CdS	Cadmium sulphide
CdTe	Cadmium telluride
BSF	Back Surface Field
$V_{oc}$	Open circuit voltage
$I_{sc}$	Short circuit current
FF	Fill factor
eV	Electron volt

$R_{sh}$	Shunt resistance
$R_s$	series resistance
$\epsilon$	Permittivity
$\epsilon_0$	Permittivity of free space
$W$	Width of the depletion region
$V$	voltage
$q$	charge
$N_a$	acceptor concentration of p type
$N_d$	acceptor concentration of n type
$\tau$	minority charge carrier lifetime
$N_t$	defect density
$\lambda$	mean distance
$\mu$	mobility of charge carrier
$E$	electric field
$X_{p0}$	depletion layer width in the p region at thermal equilibrium
$X_{n0}$	depletion layer width in the n region at thermal equilibrium
$I_{ph}$	photo generated current
$\Phi_{ph}$	incident photon flux
$\phi_0$	barrier height in SCR
SCR	space charge region
$I_0$	reverse saturation current
$n$	diode ideality factor(IF)
$\eta$	conversion efficiency
$I$	net cell current
$G$	generation rate
$n_i$	intrinsic density of the charge carriers
$k$	Boltzmann constant
$T$	temperature in degree kelvin
FTO	Fluorine doped tin oxide
AM	Air mass

## **I. Introduction**

As the world is suffering from impending death of fossil fuels and serious pollution resulted from the fuels, solar energy is now regarded as one of the promising solution to the global energy crisis [I]. Solar energy is a free, inexhaustible resource, yet harnessing it is a relatively new idea [II]. The photovoltaic (PV) effect was first observed by Alexandre-Edmond Becquerel in 1839. Subsequently, in 1946 the first modern solar cell made of silicon which was invented by Russel Ohl. The modern photovoltaic technology is based on the principle of electron hole creation in each cell composed of two different layers (p-type and n-type materials) of a semiconductor material [III]. Solar cells can be classified into first, second and third generation cells [II]. Cadmium-Telluride (CdTe) is a semiconductor material which has various advantageous properties as compared to the other semiconductor chalcogenides of cadmium, such as comparatively great mobility, a simple controllability of the conductivity from n- to p-type, and conversely, so that cadmium telluride may be used in semiconductor devices such as crystal diodes or transistors [IV]. Thin-film cadmium telluride (CdTe) is now regarded as one of the leading materials for the development of cost-effective photovoltaic (PV) cell.

At room temperature, CdTe has a direct optical energy bandgap of 1.45 eV with a temperature coefficient of  $(2.3-5.4) \times 10^{-4}$  eV/K, which matches the solar spectrum for a photovoltaic absorber. The absorption coefficient is large, around  $5 \times 10^4 \text{ cm}^{-1}$  at photon energies 1.8 eV or greater [V, VI, VII, VIII]. CdS/CdTe based solar cell would have a theoretical photovoltaic conversion efficiency of >28% [IX]. The difference of their bandgap makes CdS suitable as window layer for CdTe Solar Cell [VII].

To regulate the performance of solar cell, different techniques are used for preparing the CdTe layer. These deposition techniques influence a variety of properties such as carrier lifetime, mobility, and absorption coefficients [X, XI]. The most efficient hetero-junction partner for the absorber CdTe in a solar cell is CdS, which is usually referred to as the window layer [VII, X, XII] because it acts a window for the light to fall on CdTe (absorber) surface.

The CdS is chosen over higher bandgap materials like ZnS or  $\text{Cd}_{1-x}\text{Zn}_x\text{S}$  as a heterojunction partner to CdTe although these can improve the window bandgap; it is because the lattice mismatch of these materials is worse than that of CdS [XIII, XIV]. To achieve CdTe cells with more efficiency, research should focus on improving the open circuit voltage ( $V_{oc}$ ),  $I_{sc}$ , and FF. One way to achieve this to reduce the back-contact barrier height [VI, XIII, XV]. All-vapor process for CdS and CdTe layers has advantages over combination processes. This is due to the elimination of waste by-products inherent in the wet process, and the facilitation of a single vacuum chamber, with neighboring deposition stations [XVI]. The CdS can be deposited on top of the CdTe in a variety of methods such as Electro Deposition, chemical bath deposition, thermal evaporation, spray, pyrolysis and sputtering [V,

XVII]. By using thermal evaporation technique, grown graphite doped CdTe/CdS thin-film heterojunction can be grown with slight increase in current amount Thus the quality of p-n junction is improved [XVIII]. The thickness of the CdS film is related to the number of incident photons that reach the CdTe. For better performance of the CdTe solar cell, the thickness of CdS layer has to be reduced, but this reduction may lead to forward leakage current to front contact through possible pinholes in CdS layer. To neutralize this unwanted forward leakage current, a high resistive buffer layer metal oxide like ZnO had been introduced in between the TCO and CdS layer [XIX]. Studies have shown that ZnO is used to improve electron extraction. It is seen that ZnO has attracted a huge attention from both basic research and industrial field. It is noted that the device with the introduction of ZnO exhibits a good lifetime and stability [XX].

.The material required for TCO should have three characteristics namely high transparency, low resistivity and good stability .The transparency should be better than 85% for wavelength 400–860 nm. It should have low resistivity on the order of  $2 \times 10^{-4} \Omega \text{ cm}$  or a sheet resistance less than 10  $\Omega/\text{square}$ . It should have good stability at the maximum temperature at which other layers are prepared. This means that no diffusion from the TCO into the layers deposited subsequently should take place [XXI]. The FTO ( $\text{SnO}_2:\text{F}$ ) films have been made from hydrofluoric acid (HF) cloud and  $\text{SnO}_2$  around  $\text{SnO}_2$  grains. The fluorine ion substitutes the  $\text{O}_2$  ion in O-Sn-O group. Fluorine has been chosen from various elements like antimony (Sb), chlorine (Cl), bromine (Br) and indium (In) for its low cost and simplicity for commercial use [XXII]. It also has better thermal stability, less expensive and low electrical conductivity ( $660\text{ohm}/\text{cm}^2$ ) as compared to ITO (Indium Tin Oxide) [XXIII]. The FTO gives extra charge carriers and localized donor levels to the conduction band, thus improving the electrical characteristics in the system [XXIV].

BSF is a buffer layer used to reduce the effect of back contact schottky barrier in the solar cell narrowing the width of the back contact schottky barrier. An important approach to overcome the barrier is to either reduce the barrier height or moderate its width by heavily doping extra layer of back surface field (BSF) with proper material between the CdTe absorber layer and final metal back contact [X]. BSF structure can be created by forming a p<sup>+</sup> layer on the back surface of an n-p. An alloy of CdTe and Te is made to get heavily p<sup>+</sup>-doped CdTe surface [XXV].

The function of back contact in CdTe solar cell is to transport holes. A high back contact barrier leads to disruption in hole transportation which in return leads to a current limiting effect called roll-over effect. At room temperature the standard back contact barrier height is 0.5eV, exceeding this value will result in reduction of the fill factor considerably [XXVI]. In this work, we excluded the investigation on back contact schottky barrier.

## II. Theoretical Background

The total photo generated current,  $I_{ph}$ , due to drift of the carrier is given by [XXVII]

$$I = qA \left[ \frac{L_h}{\tau_h} p_{NO} + \frac{L_e}{\tau_e} n_{PO} \right] (e^{qV/k_B T} - 1) - qAG(L_h + L_e) \quad 1$$

Where  $I_{ph} = qAG(L_h + L_e)$ , the photo generated current and  $I_s = qA \left[ \frac{L_h}{\tau_h} p_{NO} + \frac{L_e}{\tau_e} n_{PO} \right] 2$

For short-circuited diode,  $V=0$ , and  $I_{sc} = I_{ph} = qAG(L_h + L_e)$

$$\text{For open-circuited Diode, } I=0, \text{ and } V=V_{oc} = \frac{k_B T}{q} \ln \left[ \frac{L_h + L_e}{\left( \frac{L_h}{\tau_h} p_{NO} + \frac{L_e}{\tau_e} n_{PO} \right) G + 1} G + 1 \right] = \frac{k_B T}{q} \ln \left[ \frac{I_{ph}}{I_s} + 1 \right] \quad 4$$

Under illumination, the output power is given by [XXVII]

$$P = IV = I_s V (e^{qV/k_B T} - 1) - I_{ph} V \quad 5$$

Where  $V = \frac{k_B T}{q} \ln \left[ \frac{1 + I_{ph}/I_s}{1 + qV/k_B T} \right]$ , for maximum power output  $P_m = V_m I_m$ , where

$$V_m = \frac{k_B T}{q} \ln \left[ \frac{1 + \frac{I_{ph}}{I_s}}{1 + \frac{qV_m}{k_B T}} \right] =$$

$$V_{oc} - \frac{k_B T}{q} \ln \left[ 1 + \frac{qV_m}{k_B T} \right] \text{ and } I_m \cong I_{ph} \left[ 1 - \frac{1}{qV_m/k_B T} \right] \quad 6$$

The conversion efficiency,  $\eta = \frac{P_m}{P_{in}}$ , where  $P_{in}$  is the incident power. To maximize the output power, both  $I_{sc}$  and  $V_{oc}$  must be large [XXVII]. The term fill factor is used to define the power extraction efficiency and is expressed as

Fill Factor (FF)  $= \frac{I_m V_m}{I_{sc} V_{oc}}$ , the important figure of merit of solar cell design

In the time of illumination of a solar cell, photo generations and recombination of minority carriers happen. The following equation explains the steady state of minority carrier diffusion.

$$D_n \left[ \frac{\partial^2 (n_p - n_{p0})}{\partial x^2} + G(x) - \frac{(n_p - n_{p0})}{\tau_n} \right] = 0 \text{ and}$$

$$L_n^2 = D_n \tau_n \quad 8$$

where,  $L_n$  or  $L_e$ , diffusion length of the minority carriers;  $D_n$ , diffusion coefficient,  $G(x)$ , recombination rate;  $\tau_n$ , lifetime;  $(n_p - n_{p0})$ , the excess minority carriers density.

Maximum electric field [XXVII]

$$E = -\frac{q}{\epsilon} N_d x_{n_0} = -\frac{q}{\epsilon} N_a x_{p_0}$$

$$\text{Contact potential [XXVII]} V_0 = \frac{kT}{q} \ln \left( \frac{N_a N_d}{n_{ip} n_{in}} \right)$$

Where  $N_a$  the acceptor concentration of p is type and  $N_d$  is the donor concentration of n type.

### III. Modelling of The Solar Cell

Solar cells convert solar energy into electrical energy. When sunlight hit the solar panel and photons are absorbed by semiconducting materials, electrons are excited from their current molecular/atomic orbital. Once excited, an electron travels through the cell until it reaches an electrode. Current flows through the material to cancel the potential and this electricity is captured. The topmost layer of our simulation fabrication of the solar cell is glass, which is used to provide some support and protection to the cell. The second layer is considered as a TCO (transparent conducting oxide) layer. This layer is used to provide negative terminal of the solar cell. The layer is a trade-off between transparency and conductivity. In addition it allows passing a large spectrum of light being a high bandgap material. Fluorine-doped tin oxide (FTO) film is chosen here. Just below TCO layer, a HRT (Highly Resistive Transparent layer)/buffer layer (ZnO) has been considered to balance the voltage drop and eradicate pinhole effect. The use of buffer layer gives us freedom to decrease the thickness of the CdS layer to reduce the absorption loss and increase the  $I_{sc}$ . The window layer is the n-type semiconductor of p-n junction diode, responsible for producing the necessary potential difference across the solar cell. CdS is chosen because it has higher bandgap than CdTe and very less lattice mismatch with CdTe as compared to other materials with higher bandgap. The large optical bandgap (2.4eV) window layer is to allow energetic shorter wavelength photons to pass for the absorber layer with minimum absorption loss. The absorber layer has been kept just below the CdS layer. The p type Cadmium Telluride (CdTe) has been selected as the absorber layer considering  $1 \text{ e}10^{15} \text{ cm}^{-3}$  doping concentration.

CdTe is chosen as it has a bandgap of 1.45 eV with a temperature coefficient of  $2.3-5.4 \times 10^4 \text{ eV/K}$ , which is almost ideal for the solar spectrum. Most of the photons striking its surface have enough energy to create electron-hole pairs escaping from it to the respective terminals. This layer is made thicker so that it can absorb photons and transport charge carriers towards the terminals. Below this layer we have used a very thin BSF (Back Surface Field) layer. Highly doped p+ CdTe is chosen as BSF here. It forms n-p-p+ structure with n-CdS and p-CdTe. Thereby it narrows down the schottky barrier width between CdTe and metal back contact which subsequently

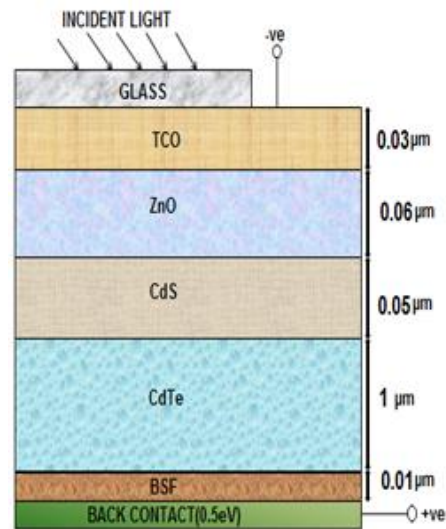
enhances the tunnelling of holes into back contact. Most of the standard metals form a barrier of around 0.5eV with CdTe. So we considered 0.5 eV back contact schottky barrier for our simulation fabrication design structure. The schematic model of the solar cell is presented in Fig1. which has been used for the simulation work.

The PC1D simulator has been used with standard resolution that is defined by is normalised error limit of  $10^{-12}$  and maximum time 60 sec. We have considered the light radiation AM 1.5G standard. The important simulation parameters are furnished in table 1.

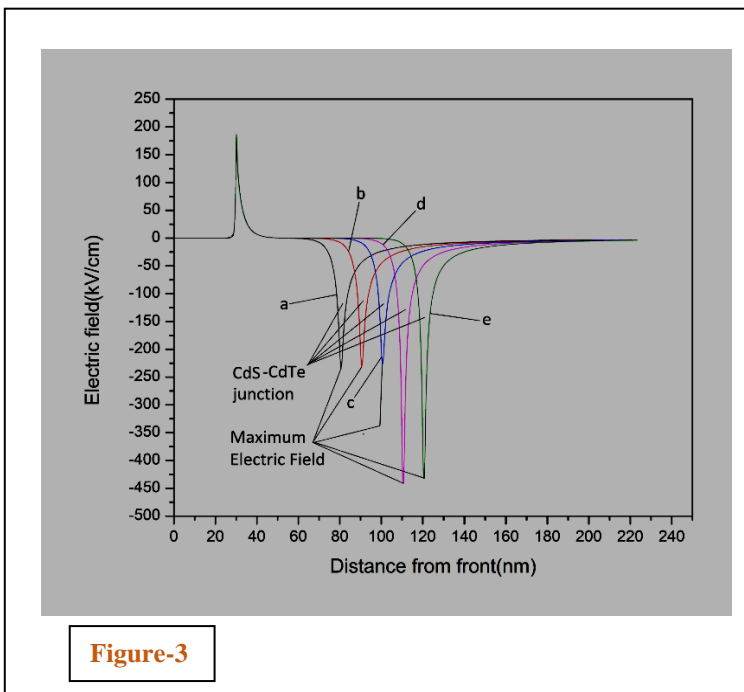
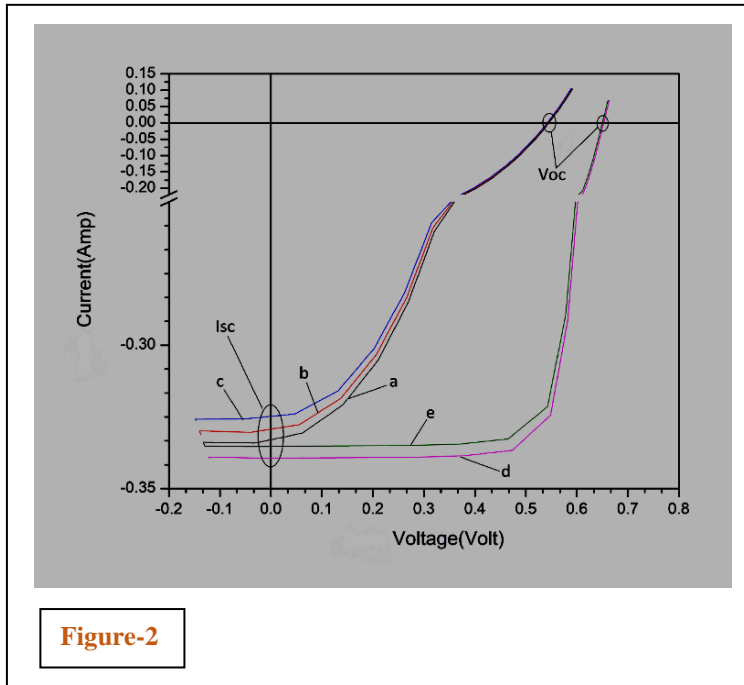
### III. Results and Discussions

All the relevant input parameters have been furnished in table-1 accordingly. Figure-2 shows the voltage-current (V-I) characteristics of the solar cell. The cell has been simulated under different thicknesses of CdS layer; however in our work we have achieved most significant performance for 0.08 $\mu\text{m}$  of CdS thickness without considering the ZnO buffer layer. The simulation results have been furnished in table-2. We have observed that upto 0.7 $\mu\text{m}$  thickness of CdS, the Voc was very poor even after getting considerable Isc. For that matter consequently we have got poor efficiency and fill factor.

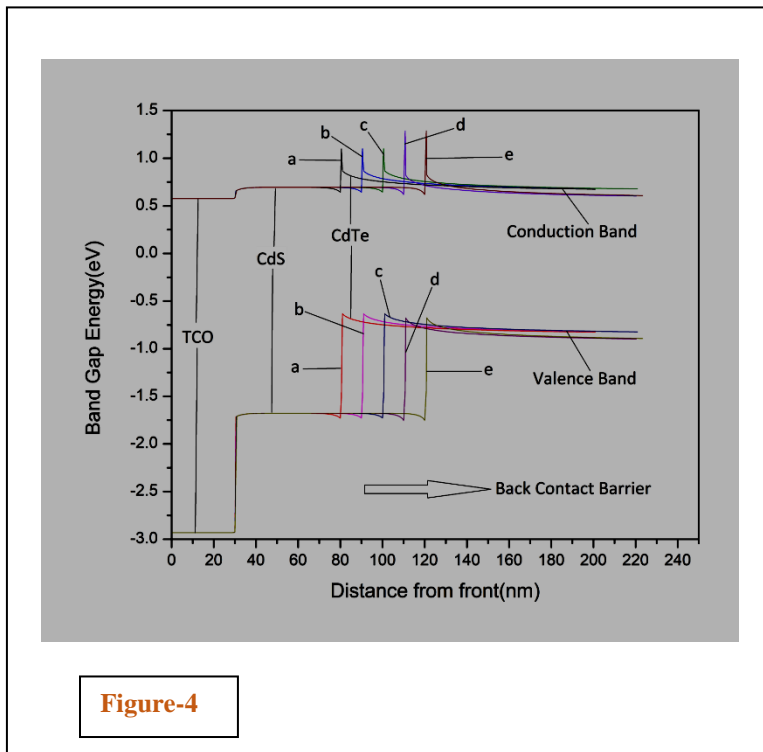
Very thin CdS layer weakens the potential drop and corresponding electric Field at the CdS/CdTe interface region (SCR), therefore cell performance gets affected. If the thickness of CdS layer is too thin then a high shunt path (like a diode or conductor) may be created between TCO and CdTe layer. As a result efficiency, Voc, and fill factor drastically get decreased. This is called pinhole effect. We have noticed these pinhole effects in case of thinner CdS (0.05 $\mu\text{m}$ , 0.06 $\mu\text{m}$ , 0.07 $\mu\text{m}$ ). Simulated results have been furnished in table-2. Figure-3 shows the electric Field distribution in the interface of CdS-CdTe junction for different thickness of CdS layer.



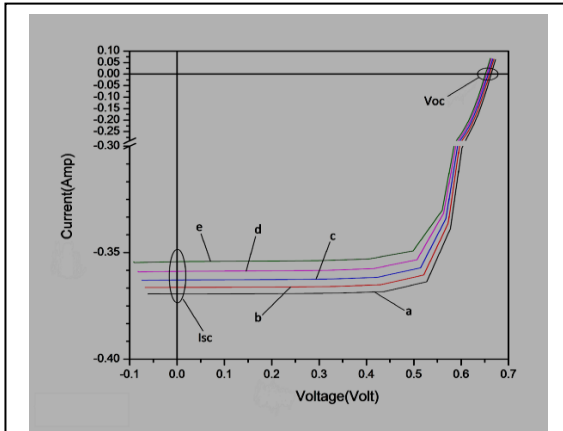
**Figure 1:** Schematic diagram of the proposed solar cell model



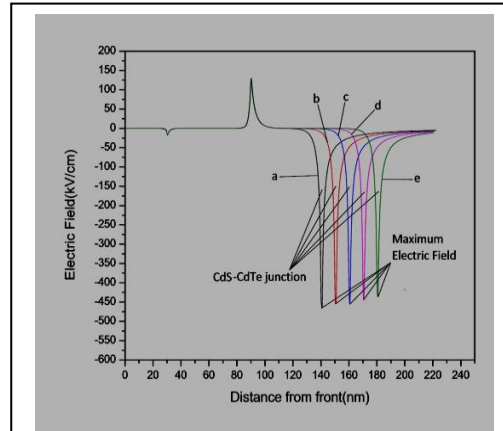




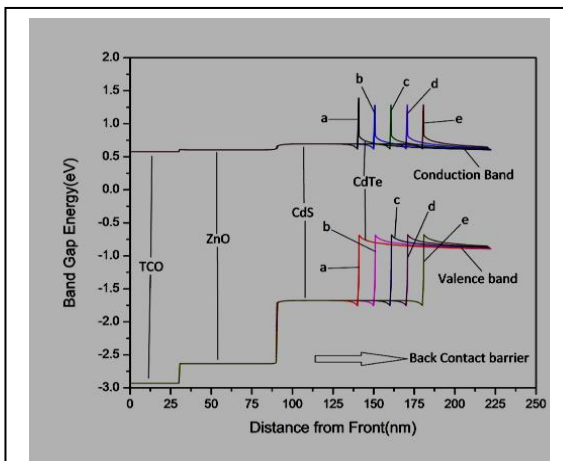
**Figure-2:** Effect of varying the thickness of CdS layer to optimize the performance of the solar cell without considering ZnO buffer layer, data considered from table-2. **Figure-3:** Electric field distribution in the interface region of CdS-CdTe junction for different thicknesses of CdS layer without considering ZnO buffer layer, data considered from table-2. **Figure-4:** Position of the conduction band and valence band at the junction of CdS-CdTe interface for various CdS layer thicknesses without considering ZnO buffer layer, data considered from table-2.



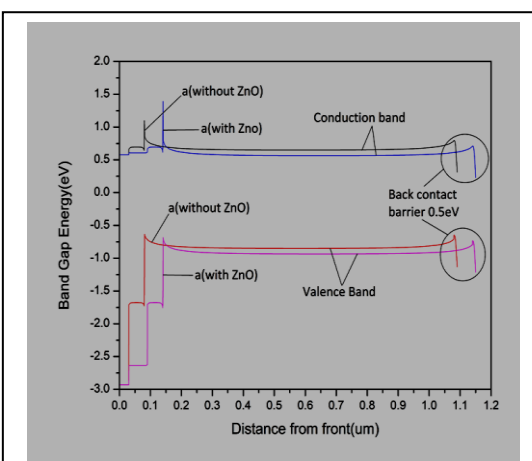
**Figure-5**



**Figure-6**



**Figure-7**



**Figure-8**

**Figure-5:** Effect of varying the thickness of CdS layer to optimize the performance of the solar cell with considering ZnO buffer layer, data considered from table-3. **Figure-6:** Electric field distribution in the interface region of CdS-CdTe junction for different thicknesses of CdS layer with considering ZnO buffer layer, data considered from table-3. **Figure-7:** Position of the conduction band and valence band at the junction of CdS-CdTe interface for various thicknesses of CdS layer with considering ZnO buffer layer, data considered from table-3. **Figure-8:** Comparison between two investigations (with ZnO buffer layer & without ZnO buffer layer) on conduction band and valence band position for very thin CdS layer thickness (0.05 $\mu$ m), data considered from table-2 and table-3.

Due to pinhole effect (thinner CdS: 0.05 $\mu$ m, 0.06 $\mu$ m, 0.07 $\mu$ m), the electric fields have become very poor (a, b, c). In this case for thicker CdS layer (80nm), we have observed better electric field which eventually improves the cell performance (label d of figure 2-4, table 2). The thicker window layer creates a strong grain boundary at CdS/CdTe interface preventing pinhole effectively. Similarly, if we follow the band diagram in figure-4; we can see that due to the effect of the electric field at CdS/CdTe interface, the peak of label a (very thin, 50nm CdS) curve is the worst among all the peaks at conduction band edge. So formation of pinhole significantly affects the band diagram. In order to overcome pinhole effect we have inserted a Highly Resistive Transparent (HRT) layer (ZnO) between TCO and CdS layers in our simulation fabrication.

The investigation results after insertion of the ZnO have been furnished in table-3. Without inserting ZnO between TCO and CdS layer, we achieved worst cell performance at 0.05 $\mu$ m thickness of CdS (1<sup>st</sup> Investigation, table-2). But after inserting ZnO, we have achieved best performance of the cell for the same thickness of the CdS layer. Being highly resistive, ZnO layer helps in producing very good Voc. Moreover for having high band gap, the ZnO passes large spectrum of light, because of that ZnO is called transparent layer. In addition, preventing the formation of pinholes, the insertion of the ZnO layer has been beneficial to enhance the I<sub>SC</sub>. Supporting data are furnished in table 3.

Important parameters of ZnO have been given in table-1 and simulated results have been furnished in table-3. After insertion of ZnO the investigations are represented by figure: 5,6,7,8. The figure 5 shows that for the thinnest layer of CdS (50nm) under the consideration, we have got the best result by successfully overcoming the pinhole effect which was the worst in the case of without ZnO (label a of figure 2 to 4, table 3). The thinner CdS layer causes less recombination of the charge carriers, due to which we observed high I<sub>SC</sub> current, and as ZnO layer being highly resistive, the Voc has been compensated. Hence if we use ZnO, Voc gets improved which was deteriorated due to pinhole effect. In addition, we have been able to observe the impact of ZnO on band diagram (figure-7) and electric field (figure-6). Observing figure 7, it has been quite clear that a sharp peak has been developed (label a) due to the insertion of ZnO. Similarly the corresponding electric field also has been strong enough to enhance the I<sub>SC</sub> and V<sub>OC</sub> as well. In every aspect we have observed the best results (label a in figure-5, 6, 7) for the thinnest CdS layer (0.05 $\mu$ m) under the consideration. In these investigations, we also have noticed that as the thickness of CdS layer increases the cell performance gets decreased. This is to say that due to increase in thickness of CdS layer, the absorption and recombination in this layer have been increased, which subsequently affects the cell performance. In figure-8, we have presented a comparison between band diagrams of label "a" of figure 4 and figure 7 to draw a justified comparison between with and without ZnO insertion for 50 nm thickness of the window layer. In this case it is clearly understood that with the use of ZnO, good cell performance can be achieved even with the use of very thin

CdS layer. The results have been directly reflected in table-3. It has been observed that ZnO buffer layer influences the conduction band to be shifted down which may be effective further to compensate the reduction of charge carrier collection due to back contact schottky barrier. We have excluded the investigation on the schottky barrier in this work.

**Table-1: Input parameters used**

Layers	Doping Concentration (cm <sup>-3</sup> )	Bulk Recombination (ns)	Thickness (μm)
TCO	1e10 <sup>20</sup>	0.1	0.03
ZnO	1x10 <sup>19</sup>	1	0.06
CdS	1x10 <sup>18</sup>	1	(0.05-0.09)
CdTe	1x10 <sup>15</sup>	1	1
BSF(CdTe++)	7x10 <sup>18</sup>	1	0.01

**Table-2: Results of the Investigations (without ZnO buffer layer) for the Figures [2-4 & 8] of labels: a, b, c, d, and e**

Figures	Thicknesses of CdS (μm)	Isc (Amps)	Voc (Volts)	Efficiency (η)	Fill Factor	Maximum Electric Field (kV/cm)
<b>a</b>	0.05	0.333	0.5452	8.48%	46.70 %	236.5
<b>b</b>	0.06	0.3293	0.5436	8.38%	46.81 %	233.5
<b>c</b>	0.07	0.3248	0.5418	8.26%	46.93 %	230
<b>d</b>	0.08	0.3394	0.6526	17.84%	80.54 %	441.5
<b>e</b>	0.09	0.3353	0.6501	17.52%	80.37 %	432.5

**Table-3: Results of the Investigations (with ZnO buffer layer) for the Figures [5-7 & 8] of labels : a, b, c, d, and e**

<b>Figures</b>	<b>Thicknesses of CdS (<math>\mu\text{m}</math>)</b>	<b>Isc (Amps)</b>	<b>Voc (Volts)</b>	<b>Efficiency (<math>\eta</math>)</b>	<b>Fill Factor</b>	<b>Maximum Electric Field (kV/cm)</b>
<b>a</b>	0.05	0.3694	0.6634	19.64%	80.14 %	-467
<b>b</b>	0.06	0.3663	0.66	19.31%	79.87 %	-456
<b>c</b>	0.07	0.3629	0.657	19.00%	79.68 %	-455
<b>d</b>	0.08	0.3588	0.6541	18.68%	79.59 %	-445
<b>e</b>	0.09	0.3542	0.6514	18.49%	80.13 %	-436

#### **IV. Conclusion**

Thinning the thickness of the window layer has been an important alternative way to decrease the absorption in the window layer and enhance the  $I_{sc}$ . But it has been observed that these thinning processes create an outflow current path between absorber and TCO layers. This pinhole formation severely damages the performance of the solar cell. After investigation and analyzation of all the results, we have come to draw the conclusion that with the use of a High Resistive Transparent (HRT) layer (ZnO) between TCO and CdS layers, the affects of the formation of the pinholes for very thin window layer can be repaired.

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