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# LOW POWER OPERATION OF ANALOG ICS

**By**

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Abstract:

*A novel techniques for the operation of analog ICs at low operational voltage has been presented in this paper. Cascode techniques has been chosen as it reduces ratio errors due to input and output voltage difference. Over and above this method provides constant current over wide output voltage swing.*

**Keyword :** *analog ICs, operational voltage, voltage difference, voltage swing, constant current.*

## *¢hj§aÑ pjl (Bengali version of the Abstract)*

*HC f-œ HÉjejmjN BC-¢p …¢ml (Analog ICs) üÒf ¢œ²ujn£m ijÒV-S LjkÑ pÇfic-el SeÉ HL A¢ieh L«v-L±nm NËqZ Llj q-u-Rz LÉjp-LjXÚ (Cascode) L«v-L±nm NËqZ Llj q-u-R -k-qa¥ Cqj CeÚf¤ÉVÚ Hhw BEVÚf¤ÉVÚ ijÒVS fjbÑ-LÉl SeÉ Be¤fj¢aL œ¥¢V-L qÊÊjp L-lz p-hÑjf¢l HC fÜ¢a ijÒVS -cjm-el ¢hnjm BEVÚf¤ÉVÚ Efl phÑcj HLC ¢hcÉ¥v plhljq L-lz*

## Introduction :

Running circuits with reduced supply voltage is of great advantage with the demand of low power application[1]. In an electronics circuit, power dissipation is of two kind namely, static power dissipation and dynamic power dissipation. In CMOS devices power dissipation occurs due to logic transitions and supply voltage variations. So on reduction of supply voltage, saving in power dissipation occurs. If supply voltage is reduced, noise margin will

reduce by keeping threshold voltage remaining same. For improving noise margin, sub threshold leakage current will increase exponentially with the reduction of threshold voltage. So the devices need to be designed to have threshold voltages that maximize net reduction in dissipation. Power delay product of CMOS devices decreases with the reduction of supply voltage and delay increases monotonically. Power delay product is also a function of width - to - length ratio of the devices[2]. So from the power delay product considerations both supply voltage and width to length ratio of the devices are to be considered.

Total power dissipation in CMOS circuit incorporates dynamic and static portion during active mode of operation. For standby mode, power dissipation is due to standby leakage current. For dynamic power dissipation, there are two components; one from the switching part due to charging and discharging load capacitance and the other is short circuit power due to nonzero rise and fall time input waveforms. Static power is determined by leakage current through each transistor and dynamic power is determined by switching activity, operation frequency, load capacitance, and supply voltage

**Mathematical relation is,**

$$P_{D=\propto fc V_{dd}^2} \quad (1)$$

$$P_{leak} = I_{leak}.V_{DD} \quad (2)$$

**Where:**

$\propto$= switiching activity; f= operation frequency, c= load capacitor, $V_{dd}$=supply voltage , $P_d$=Dynamic power, $P_{leak}$=Leakage Power, $I_{leak}$= Leakage Current.

**Background of the Present work:**

We know that low power operation of analog ICs mainly depend on due to logic transitions , supply voltage variation, operation frequency and load capacitance. Keeping this in mind, a novel technique is proposed in the present work where cascode current mirror technique is being adopted as because this technique reduces ratio error due to input and output voltage difference.

**Proposed system:**

The cascode type current mirror system, the small signal output resistance is much larger than normal current mirror and with the technique, ratio errors can be reduced due to difference in output and input voltages. The circuit diagram is shown below.

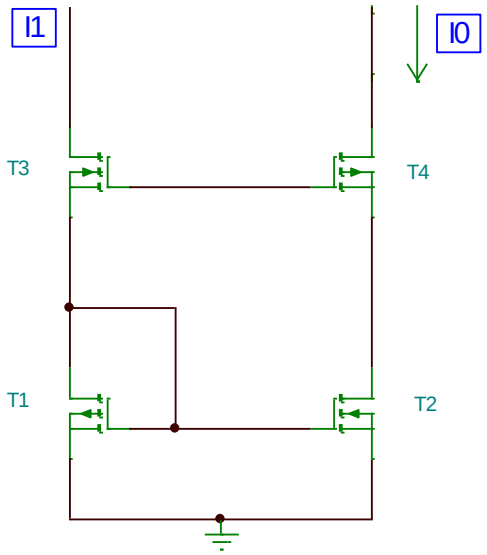

**Fig:1 : cascode type current mirror**

**The equivalent circuit of figure.1 is shown below.**

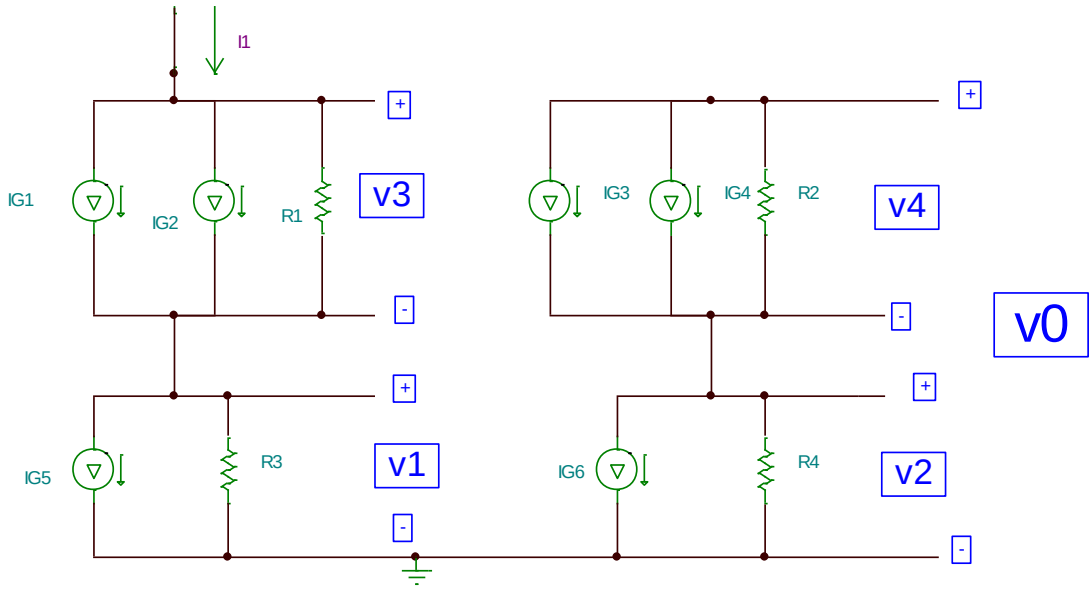


**Figure 2 small signal model of the circuit**

The output resistance

$$r_{out}=r_{ds2}+r_{ds4}+g_{m4}\, r_{ds2}\, r_{ds4}\,(1+\eta_4)$$

When, $r_{out}$ = output resistance $r_{ds2}$= drain to source résistance, $\eta_4$= constant

**Schematic Diagram:**

The schematic circuit diagram is shown in fig. 3 . In this circuit, an op- amp in inverting mode is being considered. the op-amp, taken in this circuit is LM741. Normally LM741 is being operated by ±15V power source, ±5V source is being considered and ±5V is being generated by two cascode current

mirrors. The +5V is being generated by four transistors namely M1, M2, M3 and M4 whereas -5V is being generated by using four transistor namely M5, M6, M7 and M8. The input voltage is taken a pure sine wave where amplitude is .1V

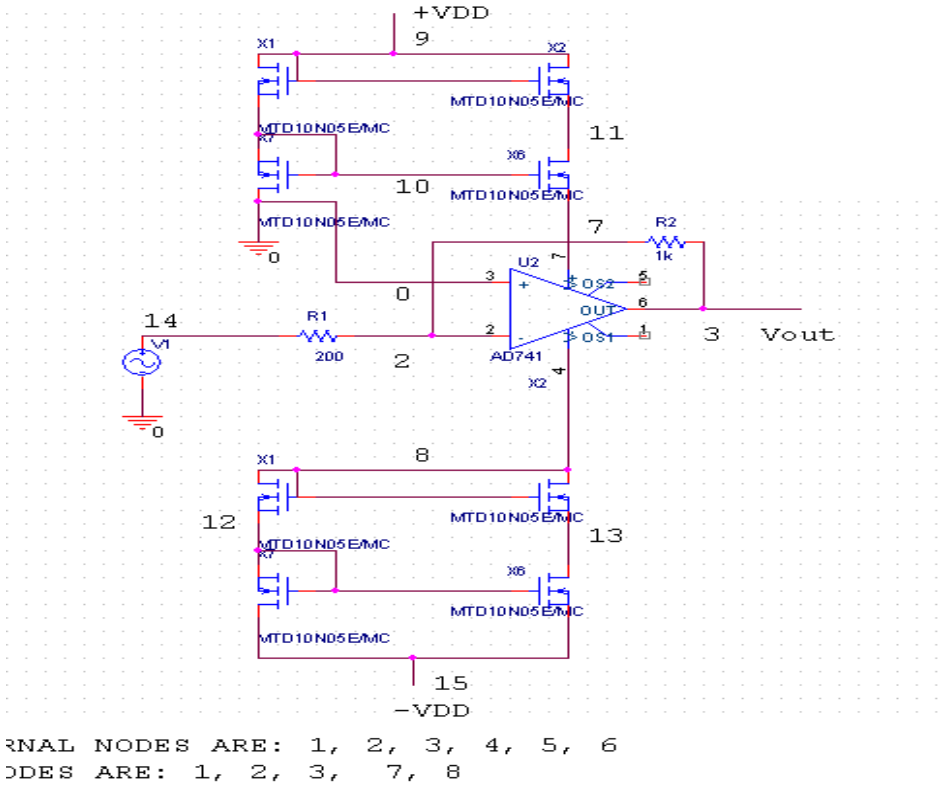


**Fig.3**

**Results and Discussions:**

The simulation results are shown below. The output results from CRO are shown in fig4. The result clearly depict that with the reduction of power sources, there is no degradation of chip performance

```
.SUBCKT OPAMP741 1 2 3 7 8

*IN(-1)   -in(=2)  out(=3)  V+ (=7)  V-(=8)

RIN 1 2 2MEG

ROUT 6 3 75

E   4 0 1 2 100K

RBW 4 5 0.5MEG

CBW 5 0 31.85nf

EOUT 6 0 5 0 1

VDD 9 0 DC 5

VEE 0 15 DC 5

M1 9 9 10 10 NM1

M2 9 9 11 11 NM2

M3 10 10 0 0 NM3

M4 11 10 7 7 NM4

M5 8 8 12 12 NM5
```

```
M6 8 8 13 13 NM6
M7 12 12 15 15 NM7
M8 13 12 15 15 NM8
.MODEL NM1 NMOS (L=5U,  w=2U)
.MODEL NM2 NMOS (L=5U,  w=2U)
.MODEL NM3 NMOS (L=5U,  w=2U)
.MODEL NM4 NMOS (L=5U,  w=2U)
.MODEL NM5 NMOS (L=5U,  w=2U)
.MODEL NM6 NMOS (L=5U,  w=2U)
.MODEL NM7 NMOS (L=5U,  w=2U)
.MODEL NM8 NMOS (L=5U,  w=2U)
.ENDS OPAMP741
VIN 14 0 SIN(0 1 1K)
R1 14 2 200
RF 2 3 1K
X1 0 2 3 7 8 OPAMP741
.TRAN 0 10m
.PROBE
END
```

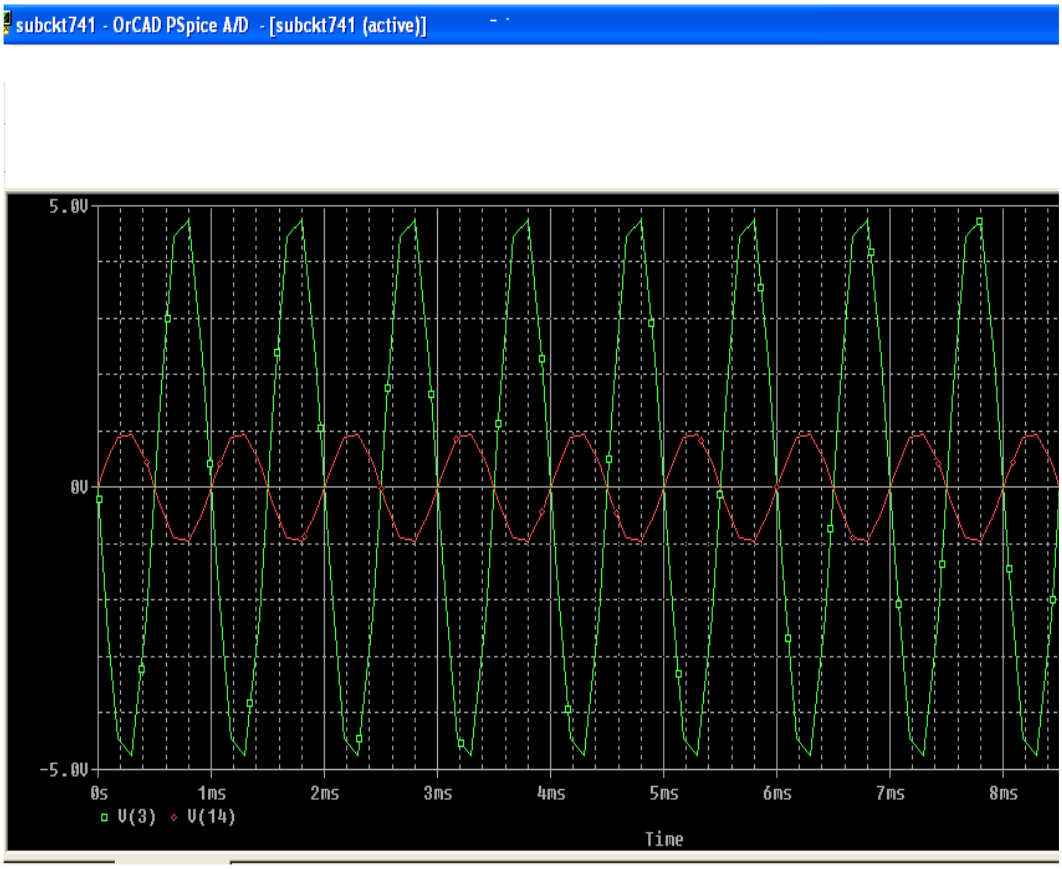


**Fig4**

## Conclusion:

Highly reliable, portable smaller integrated chips are highly desirable in semiconductor market. Mobile electronics appliances, sophisticated multimedia based electronics appliances e.g. laptop, note book, computer have enjoyed remarkable success. The most commercial design parameters for the above mentioned articles are related to power consumption. Of late in the area of portable electronic and hi performance chips, power consumptions have

emerged as a vital metric in integrated circuits and system design. Hence the technique mentioned In the research article will enable to archive the need for the common people.

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